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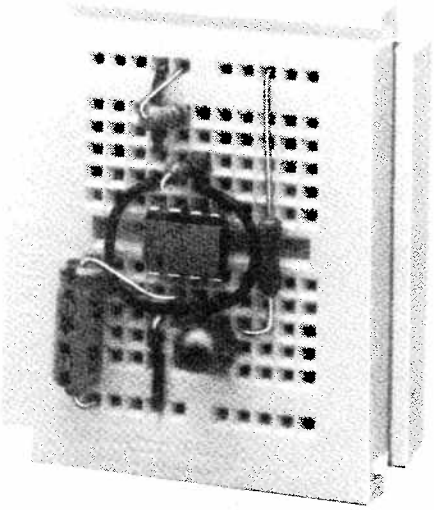
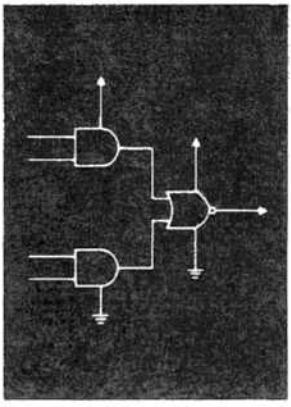
Engineer's Mini-Notebook

Digital Logic Circuits





Forrest M. Mims III

ENGINEER'S MINI-NOTEBOOK

DIGITAL LOGIC CIRCUITS

BY
FORREST M. MIMS, III

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SIXTH PRINTING - 1997

A SILICONCEPTS™ BOOK

PRINTED IN THE UNITED STATES OF AMERICA

THIS BOOK INCLUDES STANDARD APPLICATION CIRCUITS AND CIRCUITS DESIGNED BY THE AUTHOR. EACH CIRCUIT WAS ASSEMBLED AND TESTED BY THE AUTHOR AS THE BOOK WAS DEVELOPED. AFTER THE BOOK WAS COMPLETED, THE AUTHOR REASSEMBLED EACH CIRCUIT TO CHECK FOR ERRORS. WHILE REASONABLE CARE WAS EXERCISED IN THE PREPARATION OF THIS BOOK, VARIATIONS IN COMPONENT TOLERANCES AND CONSTRUCTION METHODS MAY CAUSE THE RESULTS YOU OBTAIN TO DIFFER FROM THOSE GIVEN HERE. THEREFORE THE AUTHOR AND RADIO SHACK ASSUME NO RESPONSIBILITY FOR THE SUITABILITY OF THIS BOOK'S CONTENTS FOR ANY APPLICATION. SINCE WE HAVE NO CONTROL OVER THE USE TO WHICH THE INFORMATION IN THIS BOOK IS PUT, WE ASSUME NO LIABILITY FOR ANY DAMAGES RESULTING FROM ITS USE. OF COURSE IT IS YOUR RESPONSIBILITY TO DETERMINE IF COMMERCIAL USE, SALE OR MANUFACTURE OF ANY DEVICE THAT INCORPORATES INFORMATION IN THIS BOOK INFRINGES ANY PATENTS, COPYRIGHTS OR OTHER RIGHTS.

DUE TO THE MANY INQUIRIES RECEIVED BY RADIO SHACK AND THE AUTHOR, IT IS NOT POSSIBLE TO PROVIDE PERSONAL RESPONSES TO REQUESTS FOR ADDITIONAL INFORMATION (CUSTOM CIRCUIT DESIGN, TECHNICAL ADVICE, TROUBLESHOOTING ADVICE, ETC.). IF YOU WISH TO LEARN MORE ABOUT ELECTRONICS, SEE OTHER BOOKS IN THIS SERIES AND RADIO SHACK'S "GETTING STARTED IN ELECTRONICS." ALSO, READ MAGAZINES LIKE MODERN ELECTRONICS AND RADIO-ELECTRONICS. THE AUTHOR WRITES A MONTHLY COLUMN, "ELECTRONICS NOTEBOOK," FOR MODERN ELECTRONICS.

CONTENTS

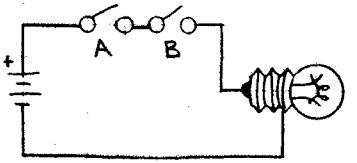
INTRODUCTION

DIGITAL ELECTRONICS IS THE TECHNOLOGY THAT MAKES POSSIBLE ELECTRONIC WATCHES, CLOCKS, CALCULATORS, COMPUTERS AND MANY OTHER DEVICES. THE CIRCUITS IN THIS BOOK PROVIDE A BASIC INTRODUCTION TO DIGITAL LOGIC AND DIGITAL ELECTRONICS. MANY OF THE CIRCUITS ARE SELF-FUNCTIONING AND REQUIRE NO ADDITIONAL COMPONENTS OR CIRCUITS. SOME CIRCUITS, HOWEVER, ARE DESIGNED TO BE CONNECTED TO OTHER LOGIC CIRCUITS. TO SIMPLIFY THIS PROCEDURE AND TO ENCOURAGE EXPERIMENTATION AND DO-IT-YOURSELF CIRCUIT DESIGN, MANY METHODS FOR INTERFACING LOGIC CIRCUITS WITH ONE ANOTHER AND WITH EXTERNAL COMPONENTS ARE INCLUDED. AS FOR THE CIRCUITS, INTERFACING AND OTHERWISE, EQUAL ATTENTION IS GIVEN TO THE TWO MOST POPULAR LOGIC FAMILIES, TTL AND CMOS. SO THE MAXIMUM NUMBER OF CIRCUITS CAN BE INCLUDED, ONLY ESSENTIAL INFORMATION IS PROVIDED. THEREFORE YOU SHOULD USE THIS BOOK IN CONJUNCTION WITH OTHER RADIO SHACK BOOKS, ESPECIALLY "GETTING STARTED IN ELECTRONICS" AND "SEMICONDUCTOR REFERENCE GUIDE."

SWITCH LOGIC

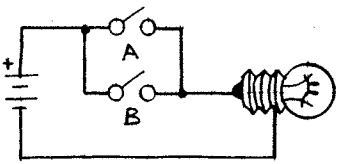
DIGITAL LOGIC CIRCUITS ARE COMPLEX NETWORKS OF TRANSISTOR SWITCHES. THE SIMPLEST LOGIC CIRCUITS ARE CALLED GATES. EXAMPLES INCLUDE:

AND GATE



A "AND" B = LAMP ON

OR GATE

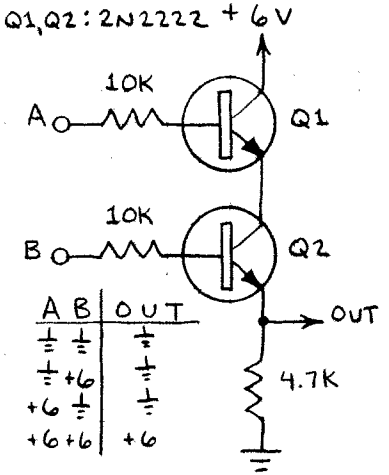


A "OR" B = LAMP ON

TRANSISTOR LOGIC CIRCUITS

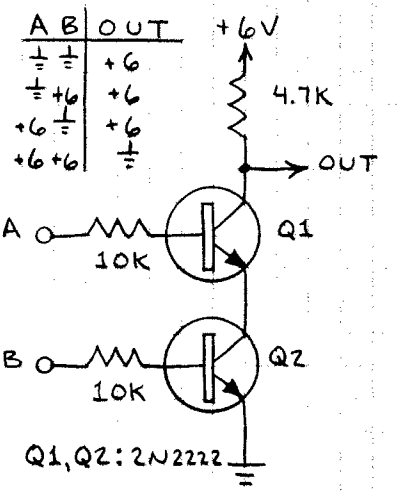
THESE CIRCUITS SHOW HOW TRANSISTOR SWITCHES CAN BE USED TO FORM FOUR OF THE SIMPLEST LOGICAL DECISION CIRCUITS OR GATES. EACH CIRCUIT INCLUDES A TRUTH TABLE THAT GIVES THE OUTPUT FOR ALL INPUT COMBINATIONS.

AND GATE



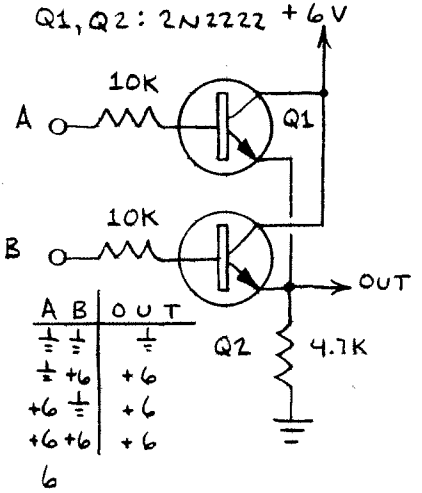
A	B	OUT
0	0	0
0	+6	0
+6	0	0
+6	+6	+6

NAND GATE



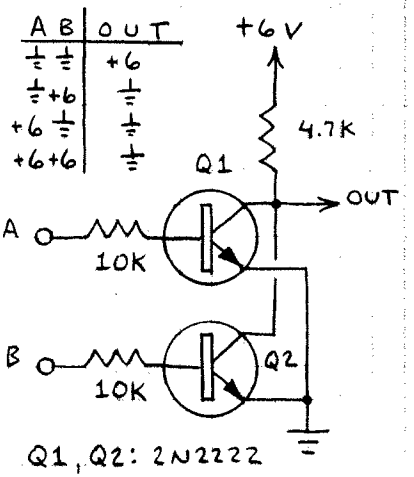
A	B	OUT
0	0	+6
0	+6	+6
+6	0	+6
+6	+6	0

OR GATE



A	B	OUT
0	0	0
0	+6	+6
+6	0	+6
+6	+6	+6

NOR GATE



A	B	OUT
0	0	+6
0	+6	0
+6	0	0
+6	+6	0

BINARY (TWO-STATE) NUMBERS

THE TRUTH TABLES ON THE FACING PAGE GIVE INPUT AND OUTPUT STATES AS +6 VOLTS AND 0 VOLTS (GROUND). THESE TWO STATES CAN BE REPLACED BY THE DIGITS 1 AND 0:

A B	AND	NAND	OR	NOR
0 0	0	1	0	1
0 1	0	1	1	0
1 0	0	1	1	0
1 1	1	0	1	0

THE SEQUENCE OF INPUTS FORMS THE FIRST FOUR NUMBERS IN THE BINARY SYSTEM.

OTHER 2-INPUT LOGIC GATES INCLUDE:

A B	EXCLUSIVE OR	EXCLUSIVE NOR
0 0	0	1
0 1	1	0
1 0	1	0
1 1	0	1

A BINARY DIGIT (0 OR 1) IS CALLED A <u>BIT</u>. PATTERNS OF BITS CAN REPRESENT DECIMAL NUMBERS, LETTERS OF THE ALPHABET, VOLTAGES AND OTHER INFORMATION. FOR EXAMPLE:

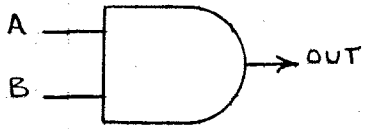
DECIMAL	BINARY	BCD
0	0 0 0 0	0 0 0 0 ; 0 0 0 0
1	0 0 0 1	0 0 0 0 ; 0 0 0 1
2	0 0 1 0	0 0 0 0 ; 0 0 1 0
3	0 0 1 1	0 0 0 0 ; 0 0 1 1
4	0 1 0 0	0 0 0 0 ; 0 1 0 0
5	0 1 0 1	0 0 0 0 ; 0 1 0 1
6	0 1 1 0	0 0 0 0 ; 0 1 1 0
7	0 1 1 1	0 0 0 0 ; 0 1 1 1
8	1 0 0 0	0 0 0 0 ; 1 0 0 0
9	1 0 0 1	0 0 0 0 ; 1 0 0 1
10	1 0 1 0	0 0 0 1 ; 0 0 0 0
11	1 0 1 1	0 0 0 1 ; 0 0 0 1
12	1 1 0 0	0 0 0 1 ; 0 0 1 0
13	1 1 0 1	0 0 0 1 ; 0 0 1 1
14	1 1 1 0	0 0 0 1 ; 0 1 0 0
15	1 1 1 1	0 0 0 1 ; 0 1 0 1

BCD IS BINARY-CODED DECIMAL. BCD PROVIDES A SHORTCUT WAY TO DISPLAY DECIMAL NUMBERS ON CALCULATOR AND WATCH READOUTS. EACH DECIMAL DIGIT IS REPRESENTED BY 4 BITS.

NIBBLE : 4 BITS
WORD : 8 BITS

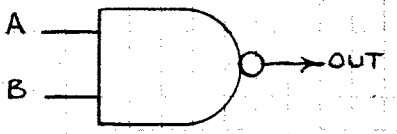
LOGIC GATES

AND GATE



A	B	OUT
L	L	L
L	H	L
H	L	L
H	H	H

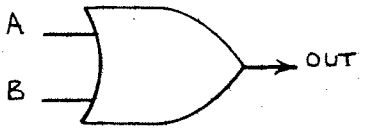
NAND GATE



A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

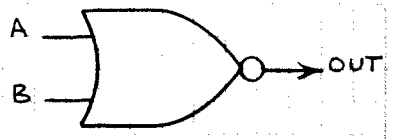
NOTE:
0 = L (LOW)
1 = H (HIGH)
L = ⏚
H = + VOLTS

OR GATE



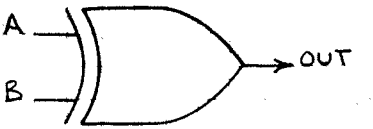
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	H

NOR GATE



A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

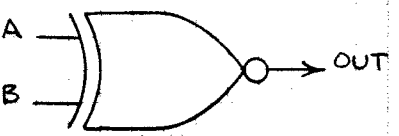
EXCLUSIVE OR



A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	L

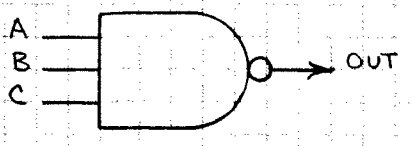
EX-OR USED FOR BINARY MATH. (COMPARE HALF-ADDER ON P. 20 WITH EX-OR ON P. 18.) BOTH USED TO COMPARE 2 INPUTS. IF EQUAL, THEN OUTPUT IS L (EX-OR) OR H (EX-NOR).

EXCLUSIVE NOR



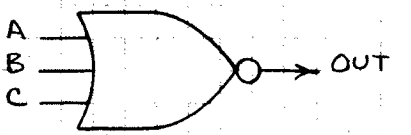
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	H

3-INPUT NAND



A	B	C	OUT
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

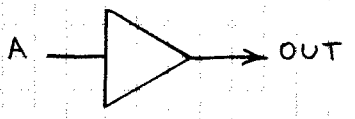
3-INPUT NOR



A	B	C	OUT
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

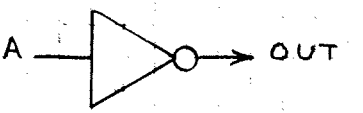
NOTE:
ADD INPUTS TO CREATE MANY NEW GATES.

BUFFER



A	OUT
L	L
H	H

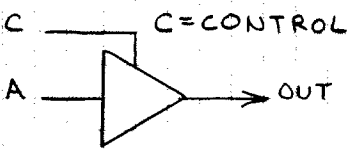
INVERTER



A	OUT
L	H
H	L

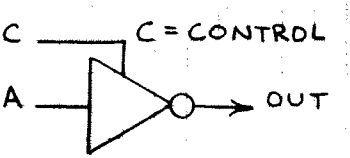
3-STATE LOGIC

BUFFER



C	A	OUT
L	L	L
L	H	H
H	X	HI-Z

INVERTER



C	A	OUT
L	L	H
L	H	L
H	X	HI-Z

TTL AND TTL/LS LOGIC FAMILIES

TTL (TRANSISTOR-TRANSISTOR LOGIC) AND TTL/LS (LOW-POWER SCHOTTKY) CHIPS ARE EASY TO USE AND REQUIRE NO SPECIAL HANDLING PRECAUTIONS. TTL CAN CHANGE STATES 20,000,000 TIMES PER SECOND. TTL USES LOTS OF POWER, AND INDIVIDUAL GATES CONSUME 3 OR MORE MILLIAMPERES. TTL/LS IS SLIGHTLY FASTER AND USES 80% LESS POWER.

OPERATING REQUIREMENTS

1. V_{cc} (POSITIVE SUPPLY) MUST NOT EXCEED 5.25 VOLTS.

2. INPUT SIGNAL MUST NEVER EXCEED V_{cc} NOR FALL BELOW GROUND.

3. UNUSED INPUTS NORMALLY ASSUME THE HIGH (H) STATE, BUT THEY MAY PICK UP STRAY SIGNALS. CONNECT THEM TO V_{cc}.

4. FORCE OUTPUTS OF UNUSED GATES H TO SAVE CURRENT. SEE TRUTH TABLES ON PP. 8-9.

5. TTL GATES CAUSE NOISE SPIKES ON THEIR POWER SUPPLY LEADS WHEN THEY CHANGE STATES. THESE SPIKES CAN BE REMOVED BY CONNECTING A 0.01 TO 0.1 μF DECOUPLING CAPACITOR ACROSS THE SUPPLY PINS OF TTL AND TTL/LS CHIPS. USE AT LEAST ONE CAPACITOR FOR EVERY 5 TO 10 GATE PACKAGES OR 2 TO 5 COUNTER AND REGISTER CHIPS. DECOUPLING CAPACITORS MUST HAVE SHORT LEADS AND BE CONNECTED FROM V_{cc} TO GROUND AS CLOSE AS POSSIBLE TO THE DECOUPLED CHIPS.

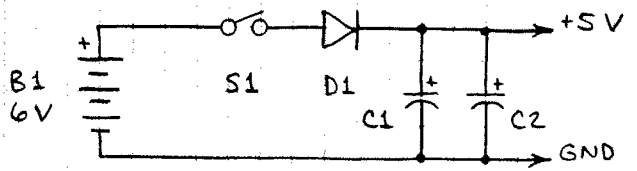
6. AVOID LONG WIRES IN TTL AND TTL/LS CIRCUITS.

7. IF THE POWER SUPPLY IS NOT ON THE CIRCUIT BOARD, CONNECT A 1 TO 10 μF CAPACITOR ACROSS THE POWER LEADS WHERE THEY ENTER THE BOARD.

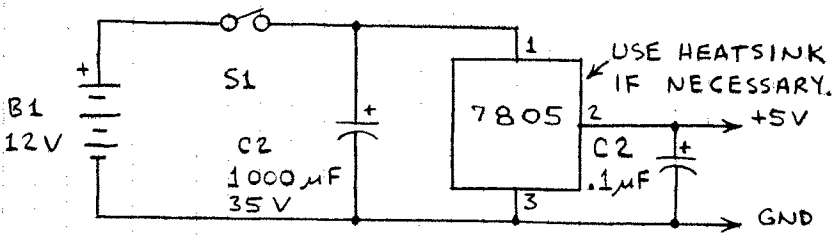
POWER SUPPLIES

TTL CIRCUITS REQUIRE A 4.75 TO 5.25-VOLT SUPPLY. BATTERIES CAN BE USED TO POWER A FEW CHIPS. OTHERWISE A LINE-POWERED SUPPLY IS MORE ECONOMICAL AND RELIABLE.

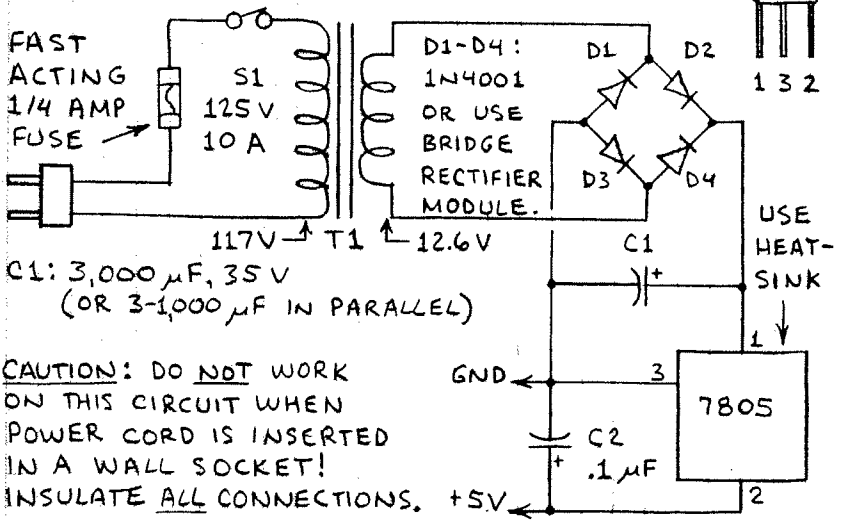
BATTERY POWER SUPPLIES



C1: 1 TO 10 μF
C2: .1 μF
D1: 1N4001



LINE POWER SUPPLY



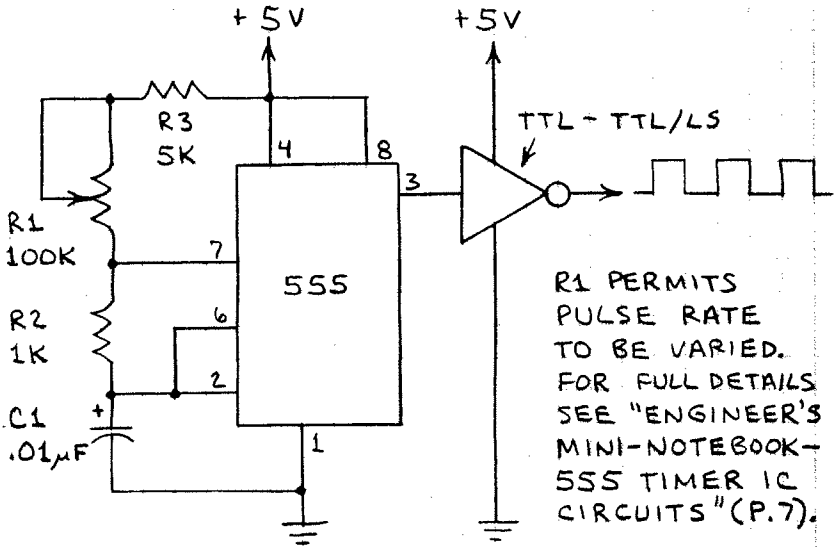
C1: 3,000 μF, 35 V
(OR 3-1,000 μF IN PARALLEL)

CAUTION: DO NOT WORK ON THIS CIRCUIT WHEN POWER CORD IS INSERTED IN A WALL SOCKET! INSULATE ALL CONNECTIONS.

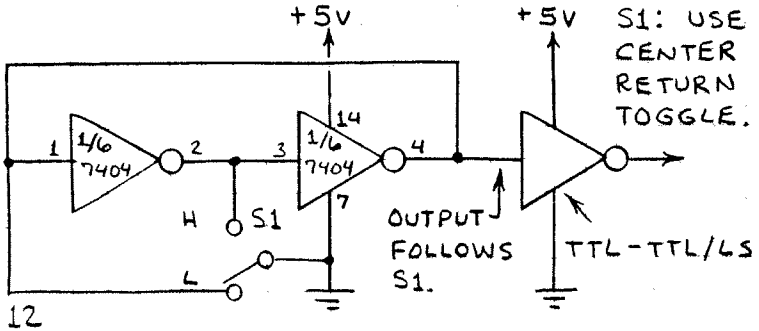
TTL INPUT INTERFACING

NON-TTL-TTL/LS CHIPS AND COMPONENTS CAN SUPPLY INPUT SIGNALS TO TTL-TTL/LS CHIPS IF THE OPERATING REQUIREMENTS ON PAGE 10 ARE OBSERVED. THE CIRCUITS BELOW SUPPLY CLEAN, NOISE-FREE PULSES TO TTL-TTL/LS CHIPS. THE INVERTER IN EACH CIRCUIT REPRESENTS A TTL OR TTL/LS INPUT.

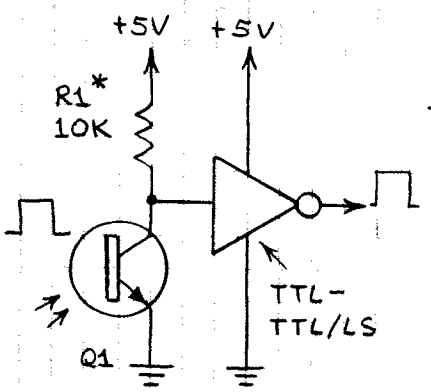
CLOCK PULSE GENERATOR

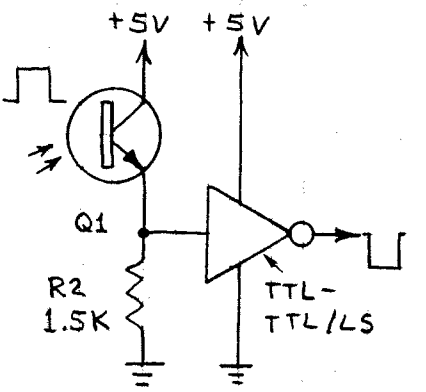


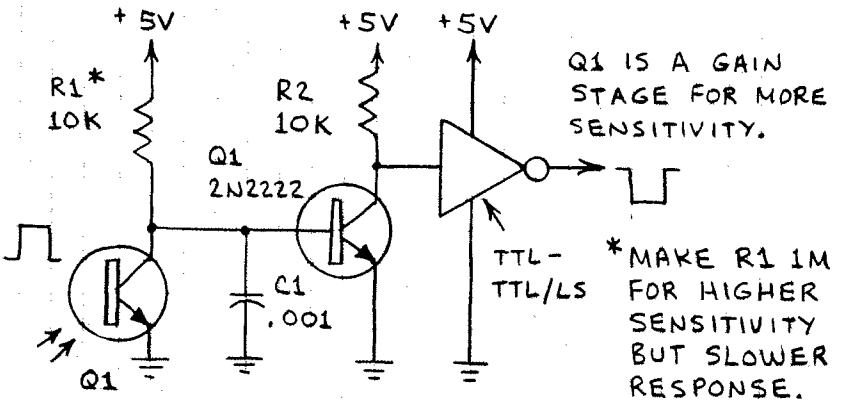
BOUNCELESS SWITCH



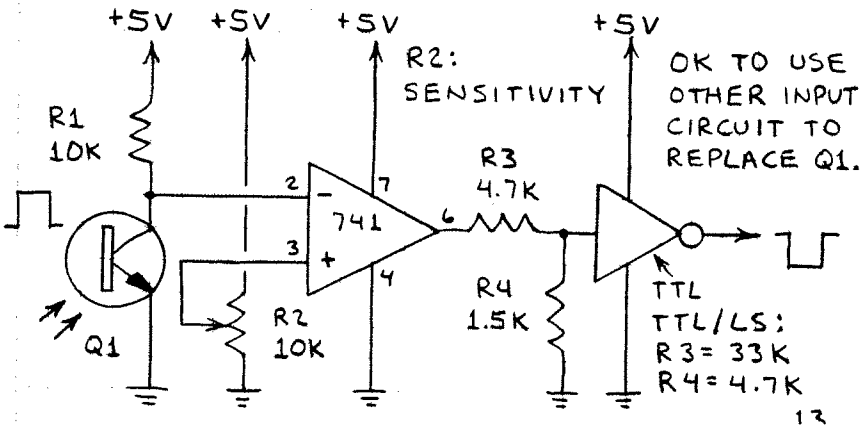
PHOTOTRANSISTOR TO TTL







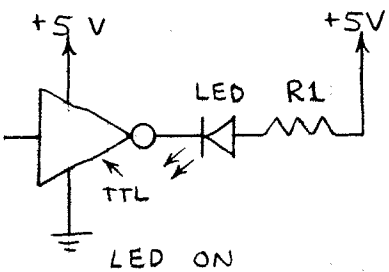
COMPARATOR/OP-AMP TO TTL



TTL OUTPUT INTERFACING

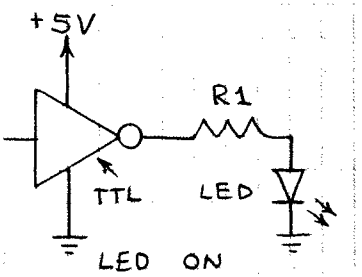
TTL CHIPS HAVE AN OUTPUT DRIVE CURRENT OF UP TO 30 MILLIAMPERES IN A SINK (OUTPUT LOW) CONFIGURATION. SEE DATA FOR SPECIFIC CHIPS.

LED DRIVERS



LED ON WHEN OUTPUT LOW.

THIS ARRANGEMENT GIVES HIGHER DRIVE CURRENT.

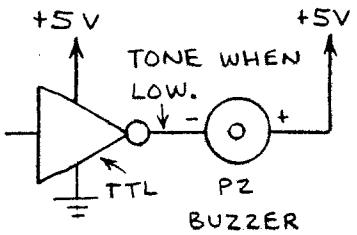


LED ON WHEN OUTPUT HIGH.

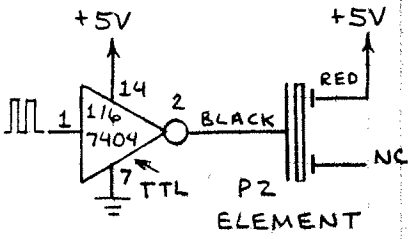
LESS DRIVE CURRENT BUT OK FOR HIGH-BRIGHTNESS LEDS.

R1 CONTROLS DRIVE CURRENT IN BOTH DRIVERS. WHEN V_{cc} = 5 VOLTS AND RED LED IS USED, R1 = 3.3/DESIRED LED CURRENT. EXAMPLE: FOR LED CURRENT OF 10 mA, R = 3.3/.01 = 330Ω.

PIEZOELECTRIC BUZZER DRIVERS

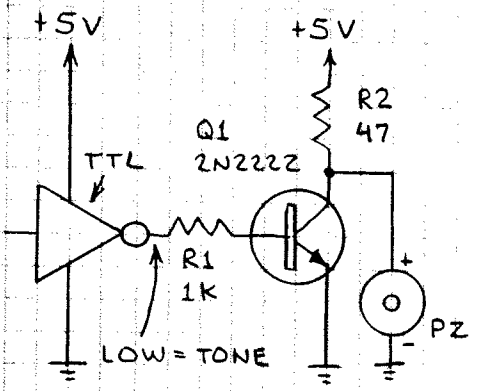


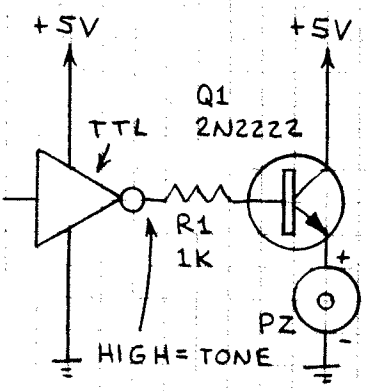
BUZZER DRIVE CURRENT SHOULD NOT EXCEED AVAILABLE OUTPUT CURRENT FROM TTL CHIP.

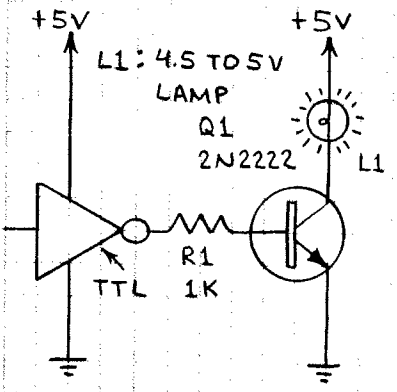


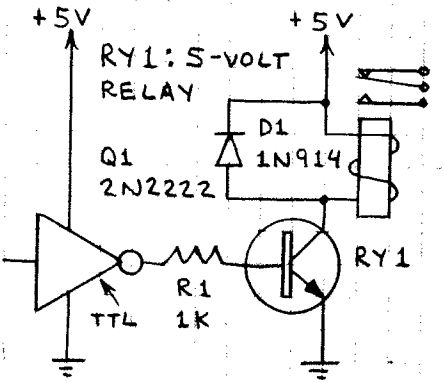
USE TO CONVERT REPETITIVE INPUT PULSES TO SOUND. ANY TTL INPUT OK.

TRANSISTOR DRIVERS

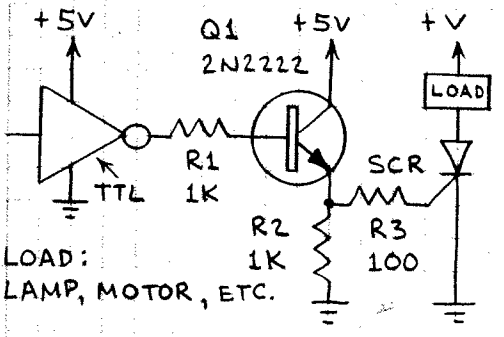


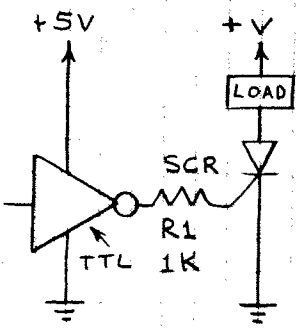






SCR DRIVERS



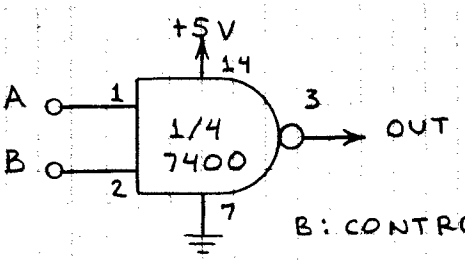


SCR SUPPLY (+V) CAN EXCEED +5V. SCR STAYS ON WHEN TRIGGERED UNLESS FORWARD CURRENT FALLS BELOW SCR HOLDING CURRENT (I_H).

TTL NAND GATE CIRCUITS

USE 7400 OR 7400LS QUAD NAND GATE. PIN NUMBERS ARE GIVEN FOR CONVENIENCE. IF DESIRED, INDIVIDUAL GATES CAN BE REARRANGED.

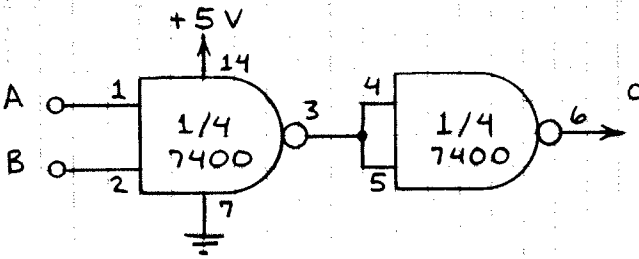
CONTROL GATE



B: CONTROL PIN.

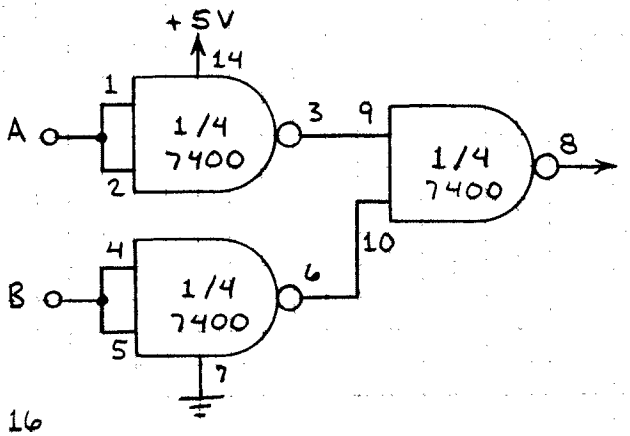
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

AND GATE



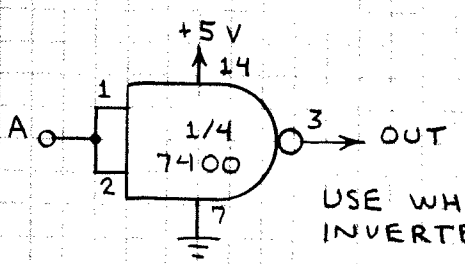
A	B	OUT
L	L	L
L	H	L
H	L	L
H	H	H

OR GATE



A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	H

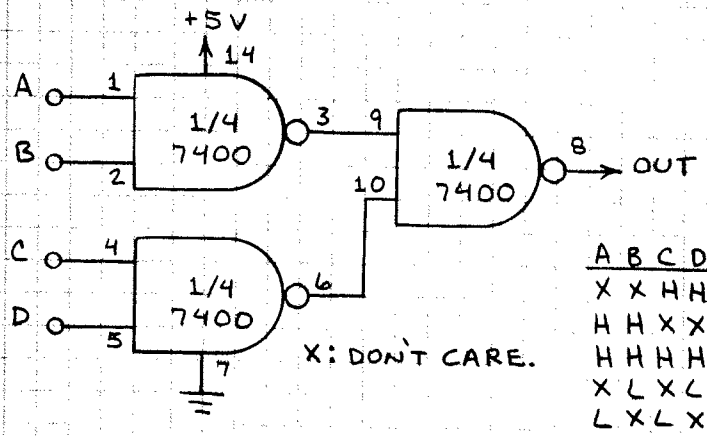
INVERTER



A	OUT
L	H
H	L

USE WHEN STANDARD INVERTER UNAVAILABLE.

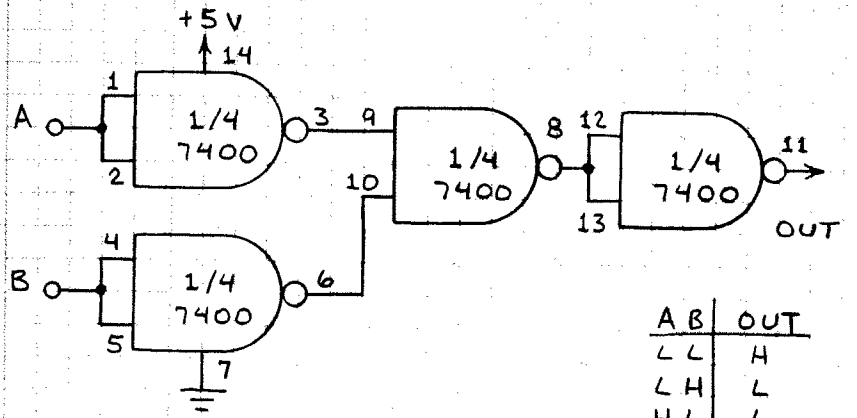
AND-OR GATE



X: DON'T CARE.

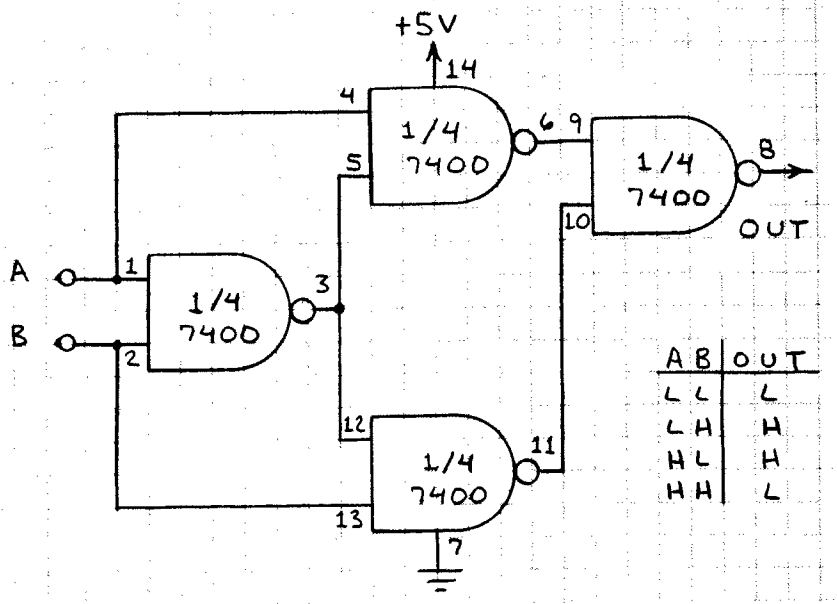
A	B	C	D	OUT
X	X	H	H	H
H	H	X	X	H
H	H	H	H	H
X	L	X	L	L
L	X	L	X	L

NOR GATE



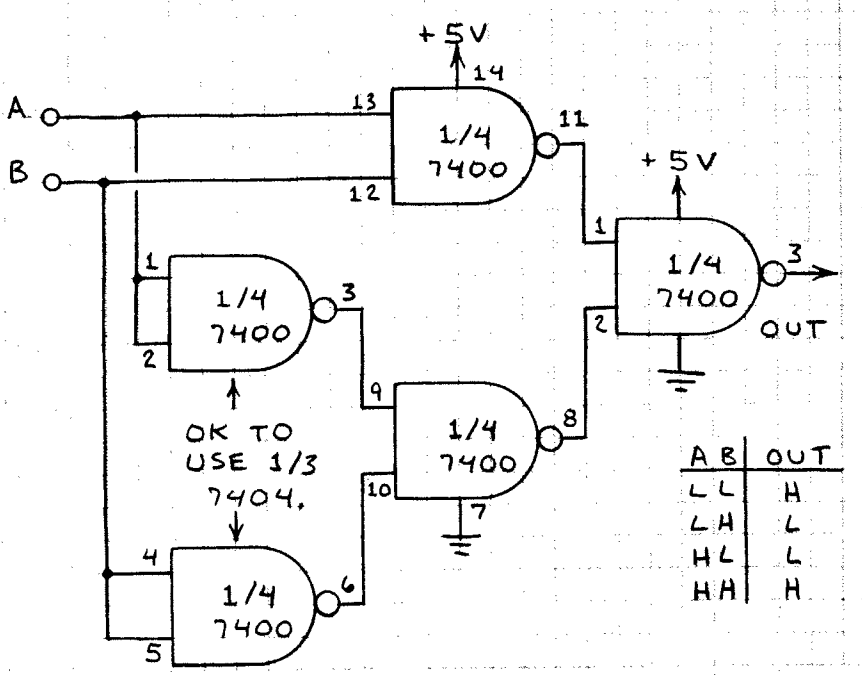
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

EXCLUSIVE-OR GATE



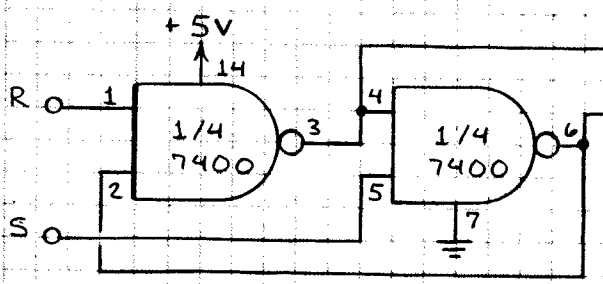
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	L

EXCLUSIVE-NOR GATE



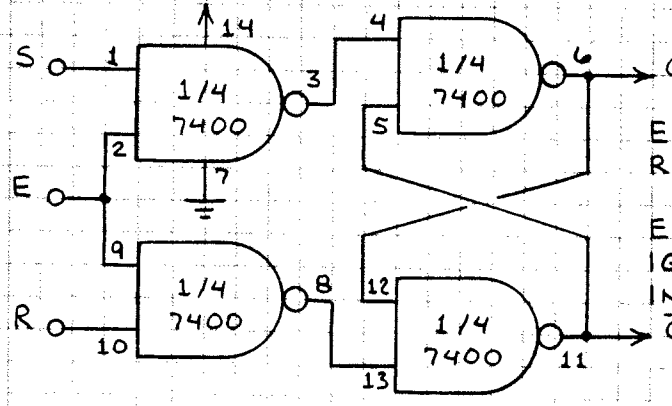
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	H

RS LATCH



R	S	Q	$\bar{Q}$
L	L	DISALLOWED	
L	H	H	L
H	L	L	H
H	H	NO CHANGE	

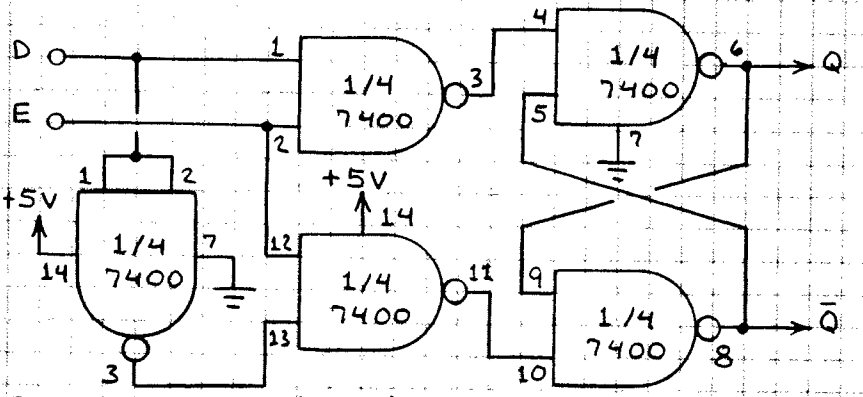
GATED RS LATCH



E = HIGH : RS LATCH.

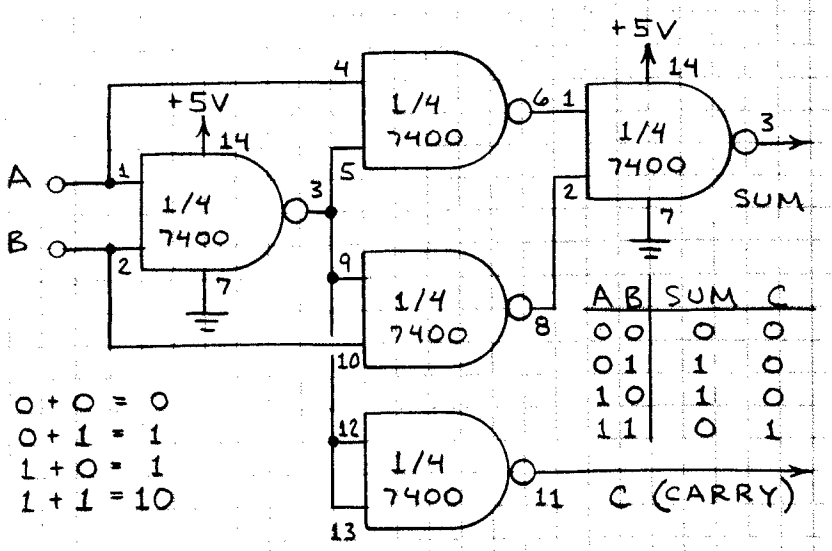
E = LOW: IGNORES INPUTS.

D FLIP-FLOP



Q FOLLOWS D (Q = D) WHEN ENABLE (E) IS HIGH. D DOES NOT CHANGE WHEN E IS LOW.

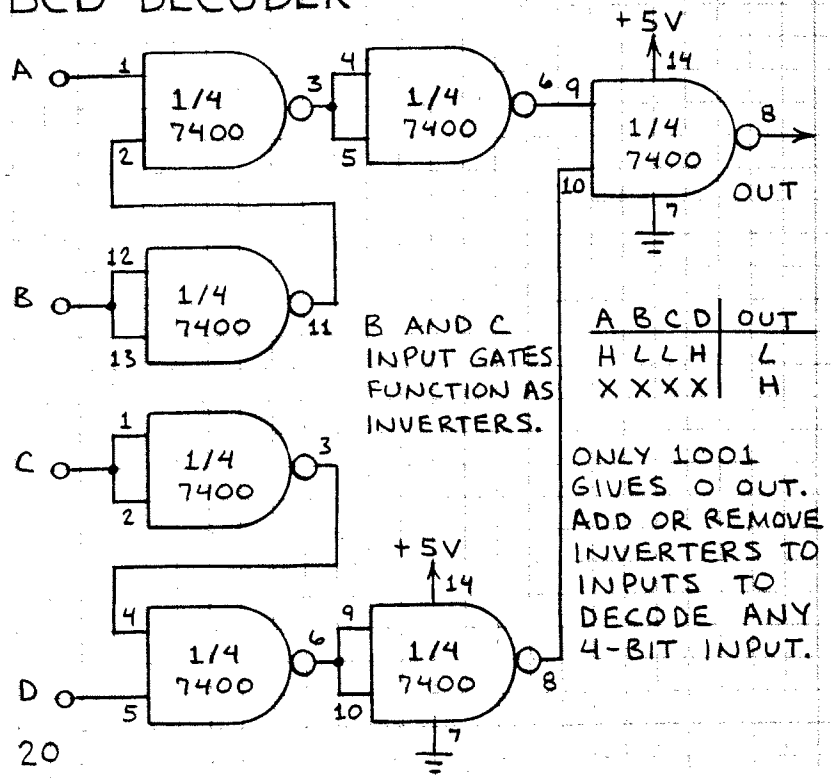
BINARY HALF ADDER



0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 10

A	B	SUM	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

BCD DECODER

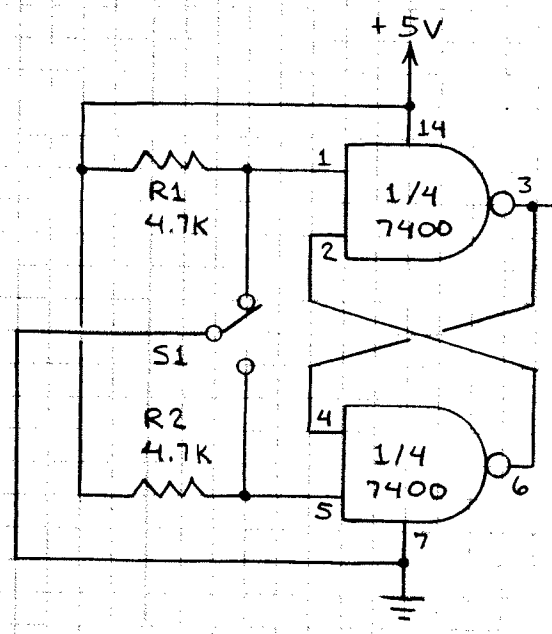


B AND C INPUT GATES FUNCTION AS INVERTERS.

A	B	C	D	OUT
H	L	L	H	L
X	X	X	X	H

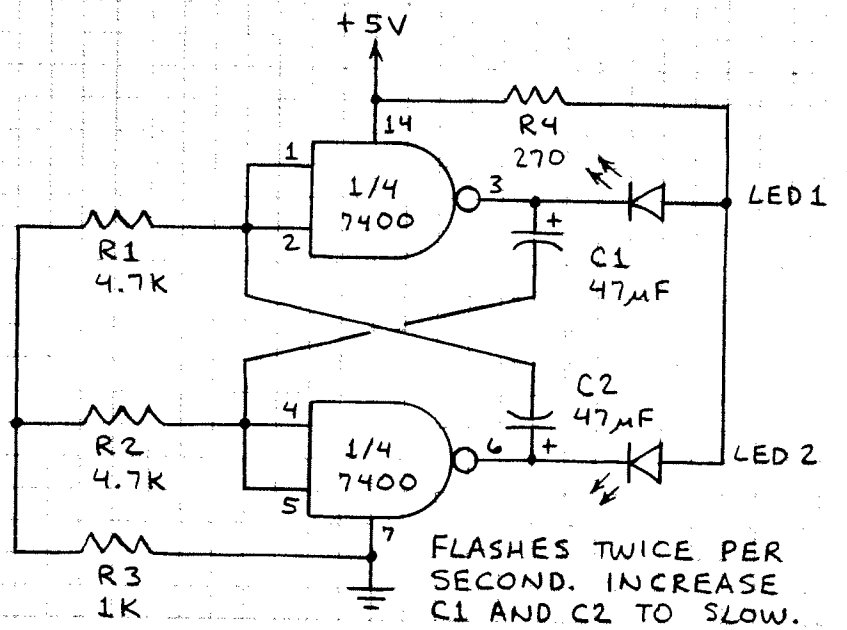
ONLY 1001 GIVES 0 OUT. ADD OR REMOVE INVERTERS TO INPUTS TO DECODE ANY 4-BIT INPUT.

SWITCH DEBOUNCER



TOGGLE S1 TO PRODUCE CLEAN, NOISE FREE PULSE AT OUTPUT. USE TO TRIGGER FLIP-FLOPS, COUNTERS, ETC.

DUAL LED FLASHER

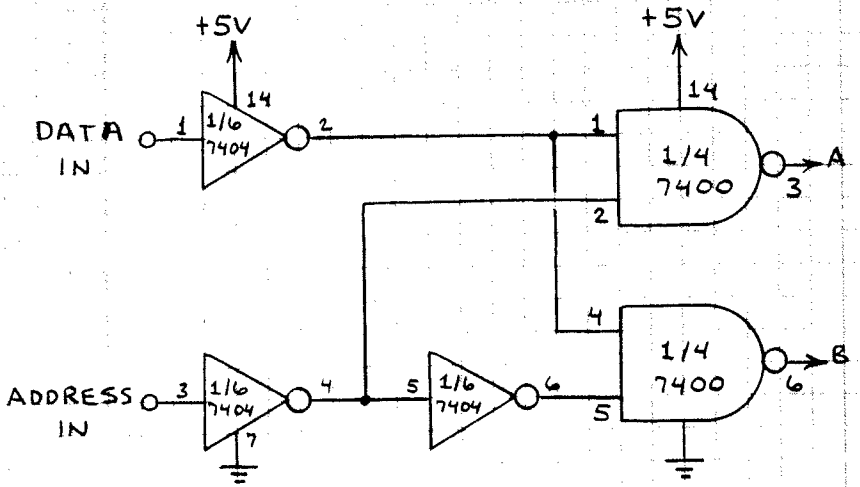


FLASHES TWICE PER SECOND. INCREASE C1 AND C2 TO SLOW.

TTL APPLICATION CIRCUITS

THE CIRCUITS THAT FOLLOW ILLUSTRATE HOW TTL CHIPS CAN BE EASILY INTERCONNECTED TO ACCOMPLISH MANY DIFFERENT APPLICATIONS.

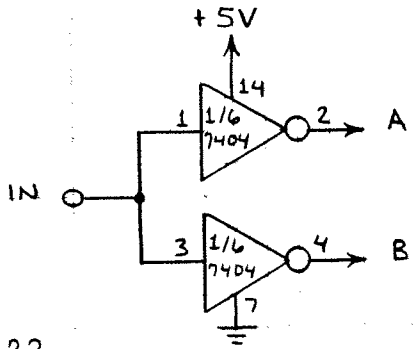
1-OF-2 DEMULTIPLEXER



INPUT BIT AT DATA IN IS STEERED TO A OR B OUTPUT BY THE ADDRESS BIT.

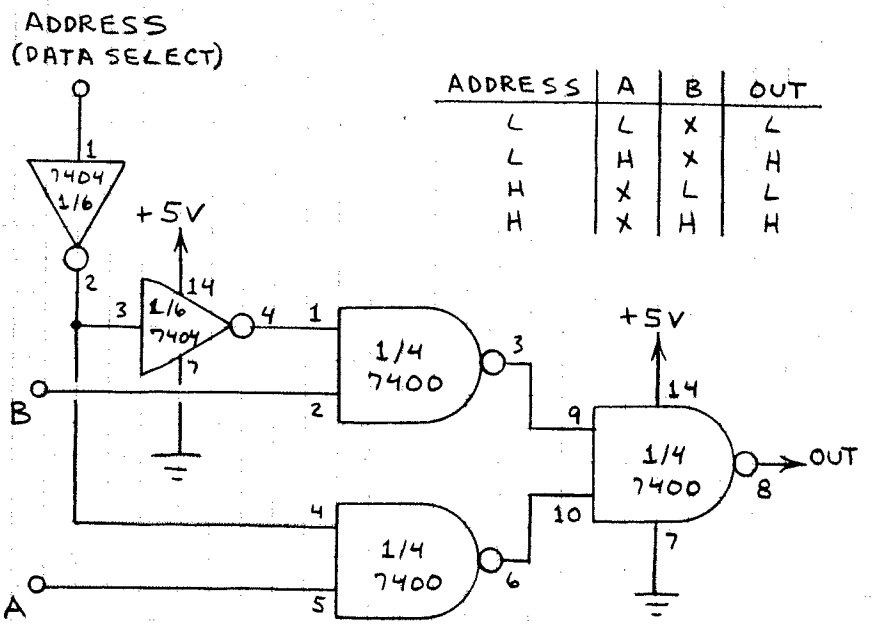
DATA	ADDRESS	A	B
L	L	L	H
H	L	H	H
L	H	H	L
H	H	H	H

EXPANDER



USE TO PROVIDE MULTIPLE OUTPUTS, EACH WITH SAME DRIVE CAPABILITY AS SINGLE OUTPUT. USE FOR LEDS, TRANSISTOR DRIVERS, ETC.

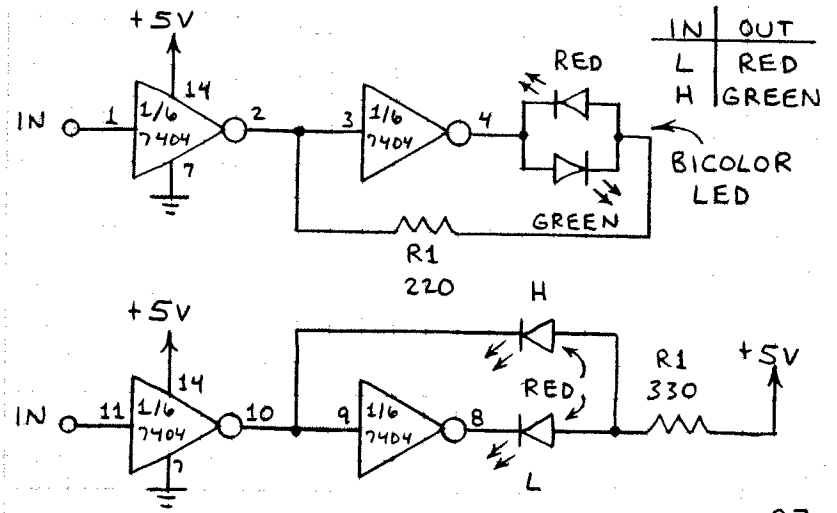
2-INPUT DATA SELECTOR



ADDRESS	A	B	OUT
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

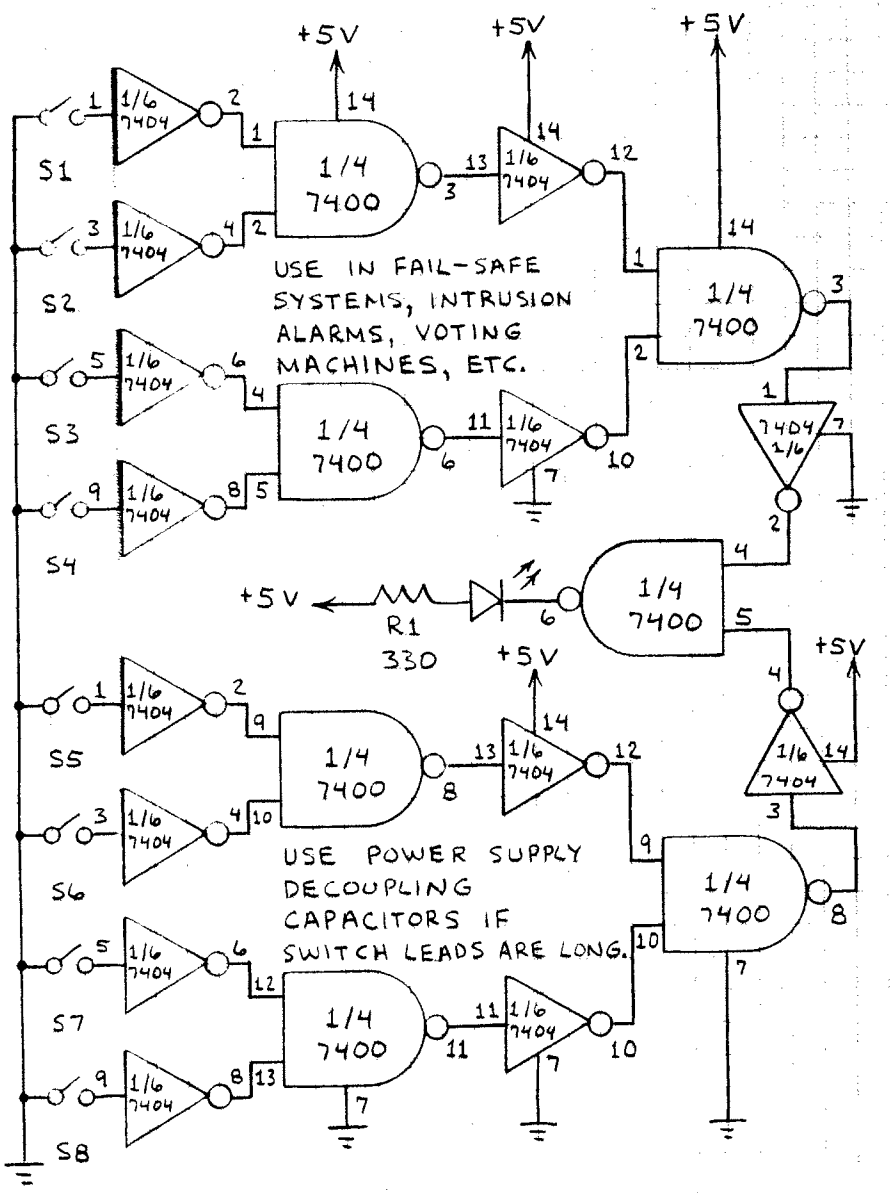
SELECTED INPUT BIT (A OR B) IS STEERED TO OUTPUT. CIRCUIT CAN BE EXPANDED.

LOGIC PROBES



IN	OUT
L	RED
H	GREEN

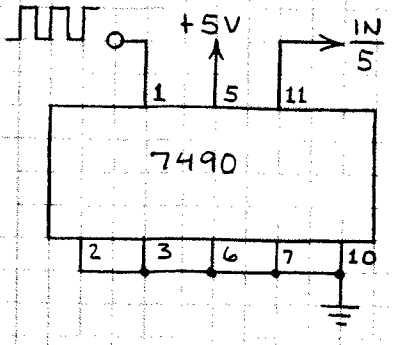
UNANIMOUS VOTE DETECTOR



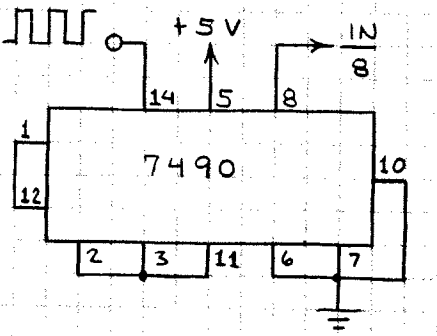
WHEN ALL INPUT SWITCHES ARE CLOSED, THE LED GLOWS. IF OUTPUT IS SENT TO OTHER LOGIC, TIE INPUTS OF 8 7404 INPUT INVERTERS TO +5V THROUGH 4.7K RESISTORS.

DIVIDE-BY-N COUNTERS

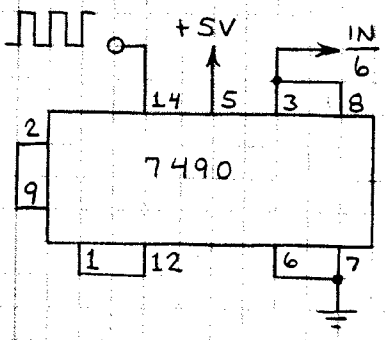
DIVIDE-BY-5



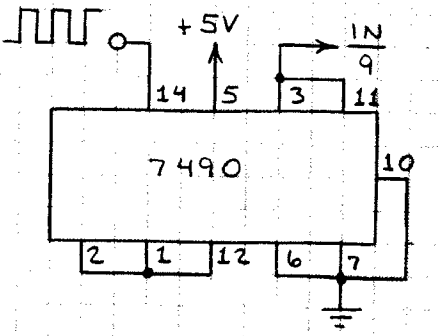
DIVIDE-BY-8



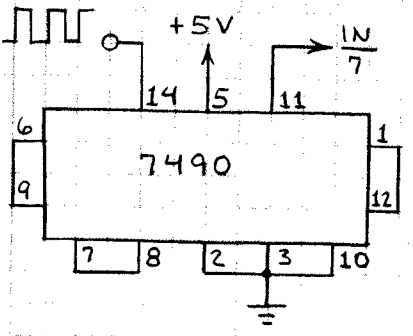
DIVIDE-BY-6



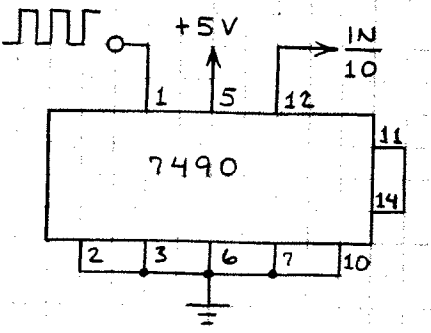
DIVIDE-BY-9



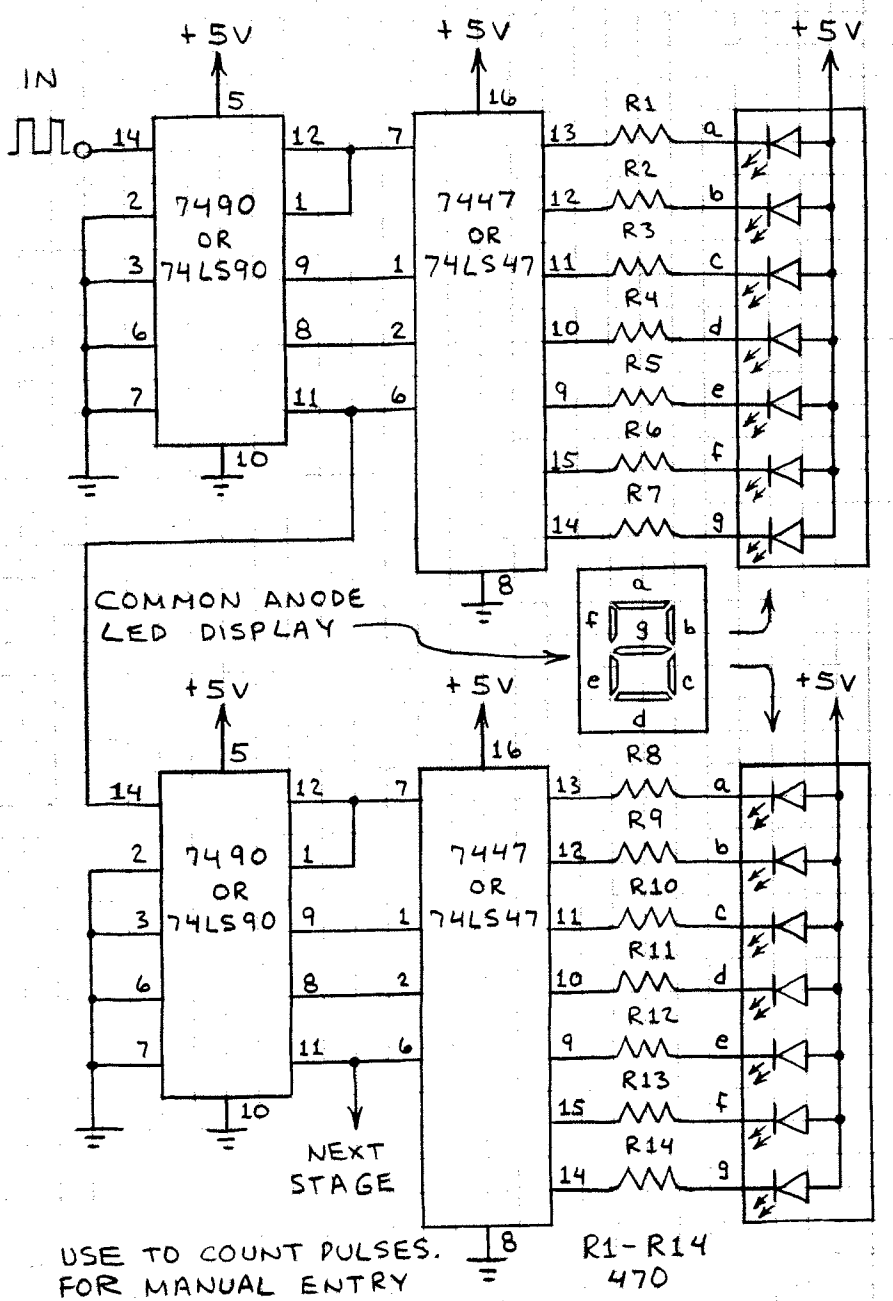
DIVIDE-BY-7



DIVIDE-BY-10

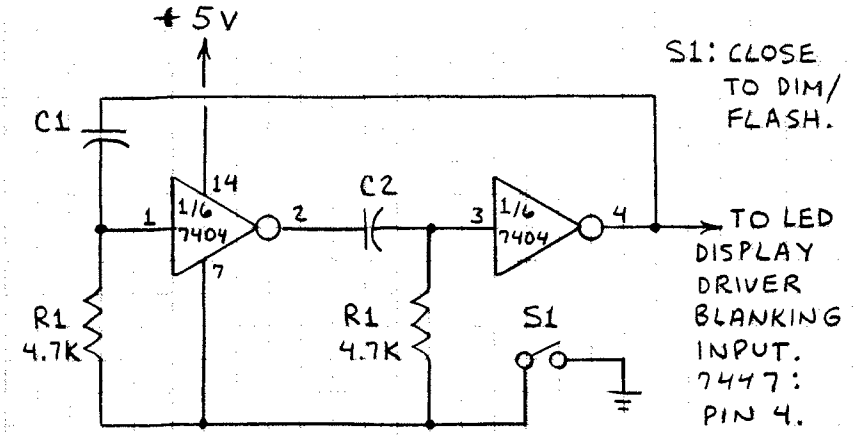


2-DIGIT BCD COUNTER



USE TO COUNT PULSES.
FOR MANUAL ENTRY
USE BOUNCELESS SWITCH.
TIMER: CONNECT 555 OSCILLATOR TO INPUT.

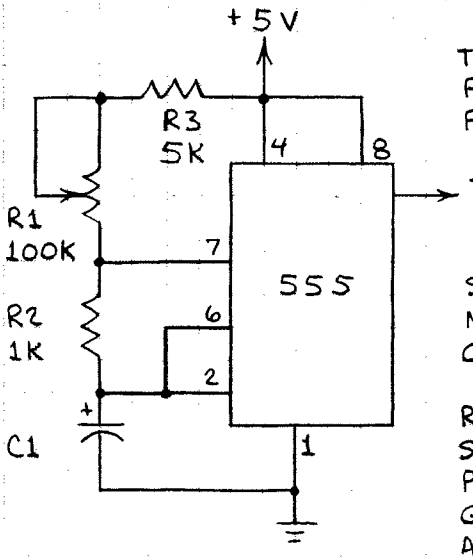
DISPLAY DIMMER / FLASHER



DIMMER : C1, C2 = 0.1 μF
FLASHER: C1, C2 = 47 μF (2 FLASHES PER SECOND)

THIS CIRCUIT WILL CONTROL 7447 DECODERS ON FACING PAGE (CONNECT PIN 4 OF EACH 7447 TO OUTPUT OF DIMMER / FLASHER).

0 TO 99 SECOND/MINUTE TIMER



THIS CIRCUIT CAN FUNCTION AS DIMMER/ FLASHER (SEE ABOVE).

TO 7490, PIN 14, ON FACING PAGE.

SECONDS : C1 = 3.3μF
MINUTES: C1 = 220μF
CALIBRATE WITH R1.

RESET TO 00: USE SWITCH TO CONNECT PIN 2 OR 3 FROM GROUND TO +5 VOLTS AND THEN TO GROUND.

CMOS LOGIC FAMILY

CMOS (COMPLEMENTARY METAL-OXIDE-SILICON) LOGIC CHIPS CAN CONTAIN FAR MORE FUNCTIONS PER CHIP THAN TTL AND TTL/LS LOGIC CHIPS. THOUGH STANDARD CMOS IS NOT AS FAST AS TTL LOGIC, IT CONSUMES CONSIDERABLY LESS POWER. A SINGLE CMOS GATE CONSUMES 0.1 MILLIAMPERE. MOREOVER, CMOS LOGIC CAN BE POWERED BY A WIDE SUPPLY VOLTAGE (3 TO 18 VOLTS). A MAJOR DRAWBACK OF CMOS IS ITS VULNERABILITY TO STATIC ELECTRICITY.

OPERATING REQUIREMENTS

1. V_{DD} (POSITIVE SUPPLY) MUST NOT EXCEED 15 VOLTS (STANDARD CMOS) OR 18 VOLTS (B SERIES).

2. INPUT SIGNAL MUST NEVER EXCEED V_{DD} NOR FALL BELOW GROUND.

3. UNUSED INPUTS WILL PICK UP STRAY SIGNALS AND CAUSE ERRATIC OPERATION AND EXCESSIVE POWER CONSUMPTION. ALL UNUSED INPUTS MUST BE CONNECTED TO V_{DD} OR GROUND.

4. IF POSSIBLE, AVOID INPUT SIGNALS THAT CHANGE STATES SLOWLY SINCE THEY INCREASE POWER CONSUMPTION. RISE AND FALL TIMES FASTER THAN 15 MICROSECONDS ARE BEST.

5. THE FREQUENCY OF THE INPUT SIGNAL MUST NOT EXCEED THE MAXIMUM OPERATING FREQUENCY OF A CMOS CHIP. A STANDARD CMOS CHIP HAS A TYPICAL MAXIMUM RESPONSE OF 1 MHz WHEN V_{DD} = 5 VOLTS AND 5 MHz WHEN V_{DD} = 15 VOLTS.

6. NEVER CONNECT AN INPUT SIGNAL TO A CMOS CHIP WHEN THE POWER IS OFF. NEVER REMOVE POWER TO A CMOS CHIP WHEN AN INPUT SIGNAL IS PRESENT.

HANDLING PRECAUTIONS

1. AVOID TOUCHING THE PINS OF CMOS CHIPS.

2. NEVER STORE CMOS CHIPS IN NON-CONDUCTIVE PLASTIC TRAYS, BAGS, FOAM, OR "SNOW."

3. PLACE CMOS CHIPS PINS DOWN ON AN ALUMINUM FOIL SHEET OR TRAY WHEN THEY ARE NOT IN A CIRCUIT OR STORED IN CONDUCTIVE FOAM.

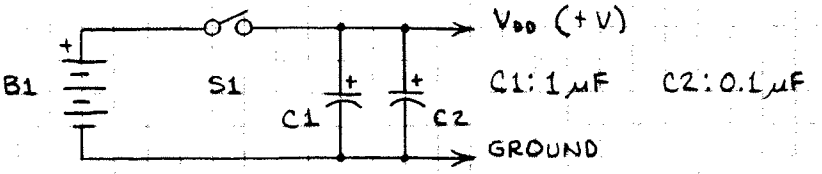
4. NEVER INSTALL A CMOS CHIP IN A CIRCUIT WHEN POWER IS APPLIED. NEVER REMOVE A CMOS CHIP FROM A CIRCUIT WHEN POWER IS APPLIED.

5. USE A BATTERY-POWERED IRON TO MAKE SOLDER CONNECTIONS TO A CMOS CHIP. AN AC POWERED IRON MAY BE USED IF THE TIP DOES NOT CARRY STRAY VOLTAGE.

POWER SUPPLIES

MOST CMOS CIRCUITS CAN BE POWERED BY BATTERIES. GENERALLY, OUTPUT DEVICES LIKE LEDS, LAMPS, RELAYS, ETC. CONSUME MUCH MORE POWER THAN THE CMOS CHIPS THAT DRIVE THEM.

BATTERY POWER SUPPLIES

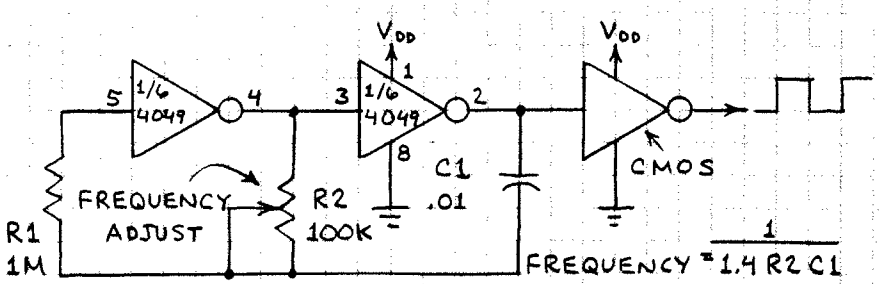


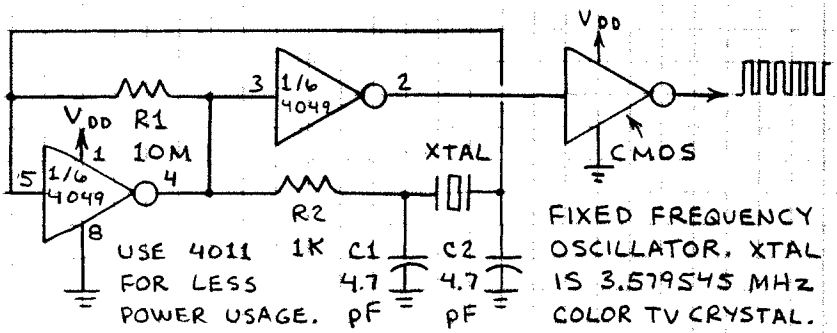
B1 IS 3 TO 15 VOLT BATTERY. C1 AND C2 ARE OPTIONAL. USE WHEN LEADS TO B1 ARE LONG. OK TO USE 7805, 7812, OR 7815 REGULATOR CHIP IN BATTERY SUPPLY ON P.11.

CMOS INPUT INTERFACING

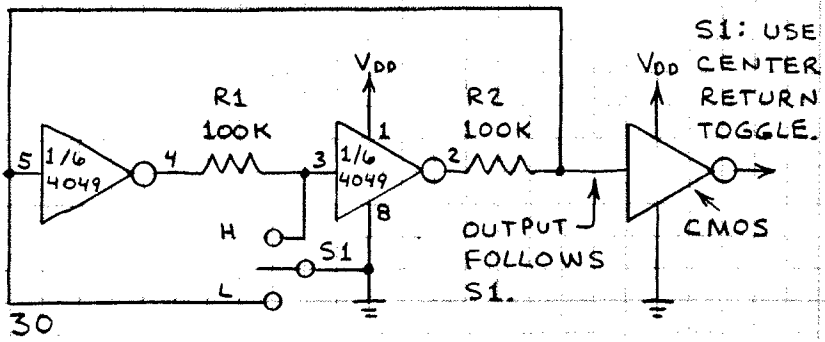
NON-CMOS CHIPS AND COMPONENTS CAN SUPPLY INPUT SIGNALS TO CMOS CHIPS IF THE OPERATING REQUIREMENTS ON PAGE 28 ARE OBSERVED. THE FINAL INVERTER IN EACH CIRCUIT BELOW REPRESENTS A CMOS INPUT.

CLOCK PULSE GENERATORS

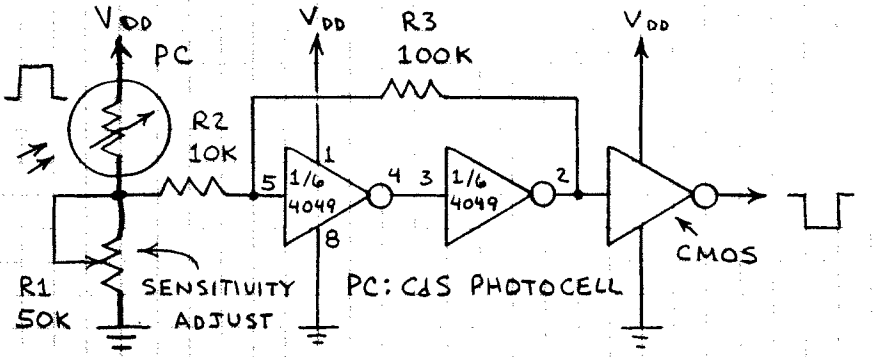




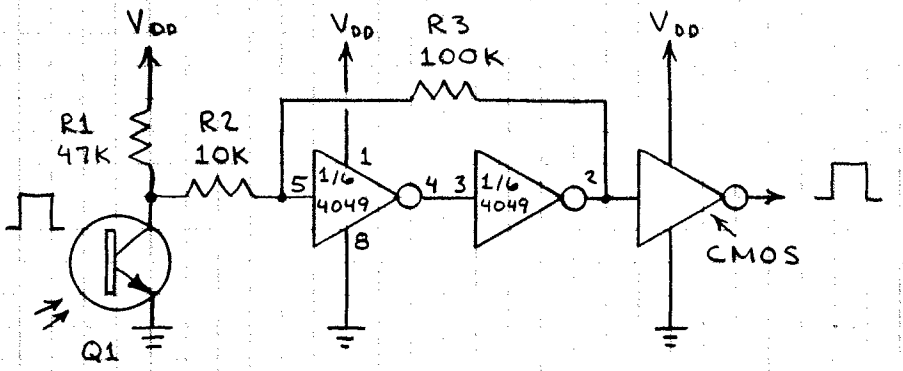
BOUNCELESS SWITCH



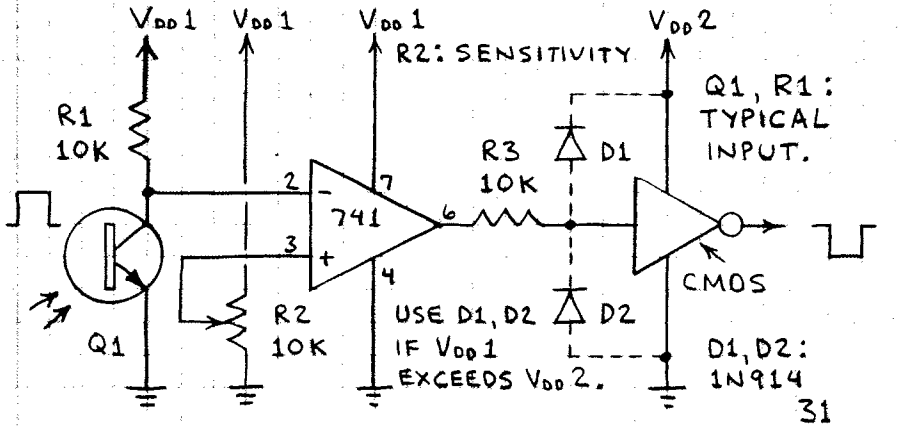
PHOTOCELL TO CMOS



PHOTOTRANSISTOR TO CMOS



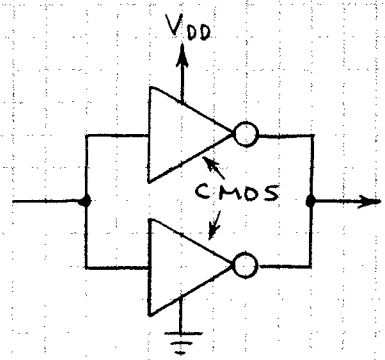
COMPARATOR / OP-AMP TO CMOS



CMOS OUTPUT INTERFACING

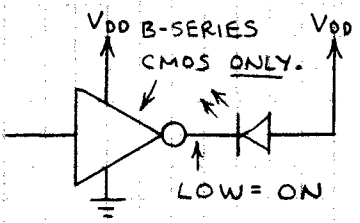
THOUGH CMOS CHIPS HAVE LIMITED OUTPUT CURRENT, MANY OUTPUT DEVICES CAN BE DRIVEN WITH THE HELP OF EXTERNAL COMPONENTS.

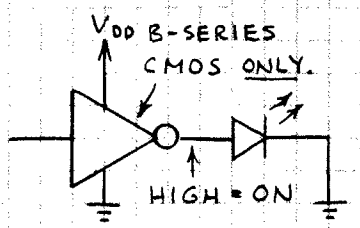
INCREASED OUTPUT



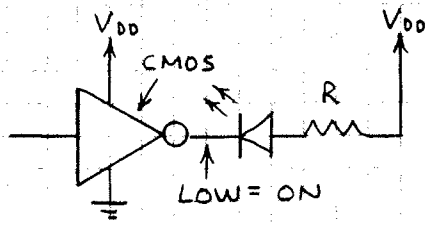
CONNECT TWO OR MORE GATES IN PARALLEL TO INCREASE OUTPUT CURRENT. TWO GATES SHOWN HAVE ABOUT DOUBLE THE OUTPUT AS A SINGLE GATE. THE 4049 AND 4050 HEX INVERTER AND BUFFER GIVE HIGH OUTPUT.

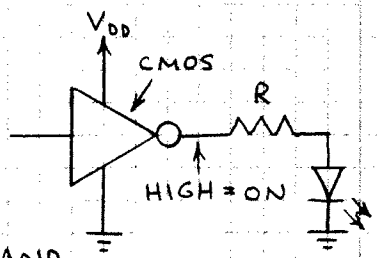
LED DRIVERS





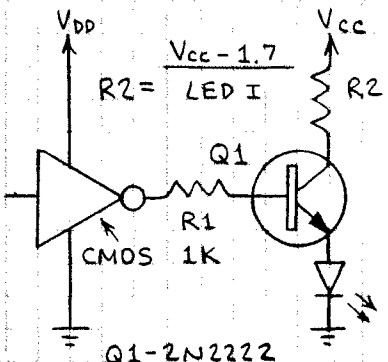
LED WITHOUT RESISTOR FOR $V_{DD} \leq 4.5$ VOLTS ONLY.

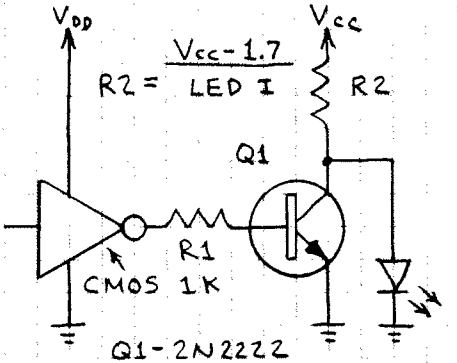


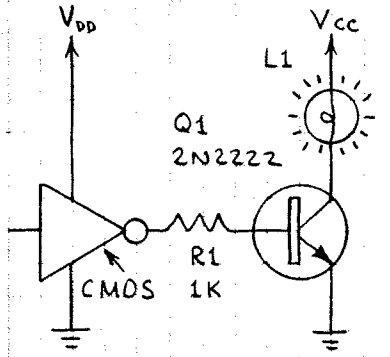


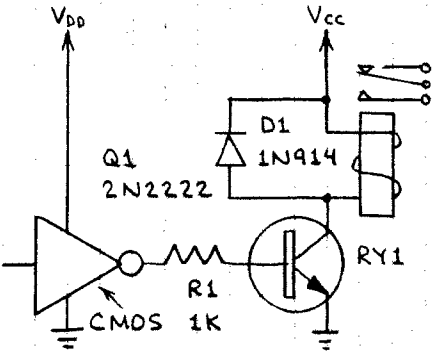
USE WHEN $V_{DD} > 6$ VOLTS AND TO SET LED CURRENT. FOR RED LED AT 10 mA (0.01A): $R = \frac{V_{DD} - 1.7}{.01}$

TRANSISTOR DRIVERS



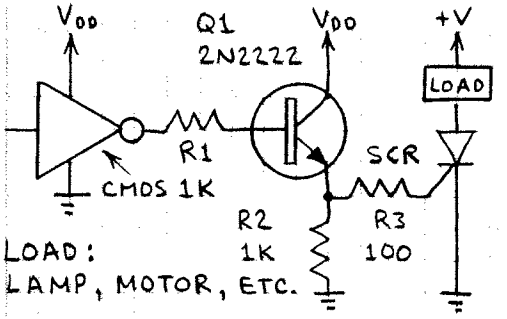


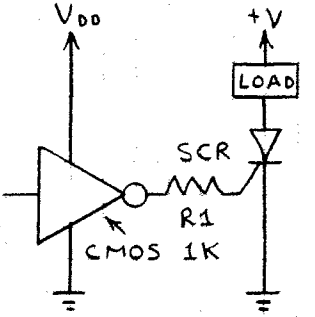




Vcc CAN BE > OR < VDD. SELECT L1 AND RY ACCORDING TO Vcc.

SCR DRIVERS



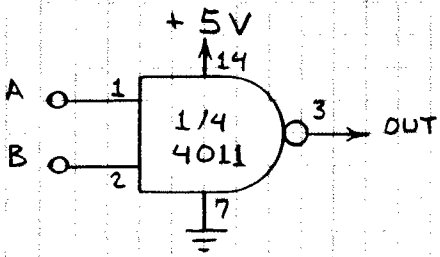


SCR SUPPLY (+V) CAN BE > OR < VDD. THESE CIRCUITS IDENTICAL TO TTL VERSIONS ON P. 15.

CMOS NAND GATE CIRCUITS

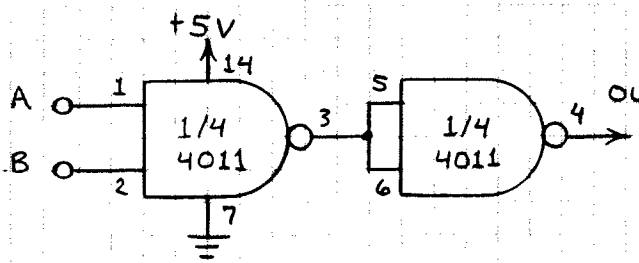
USE 4011 QUAD NAND GATE. OK TO REARRANGE GATES. ALL UNUSED INPUTS MUST GO TO V_{DD} OR GROUND. V_{DD} = +3 TO +15 VOLTS. FOLLOW CMOS HANDLING PRECAUTIONS.

CONTROL GATE



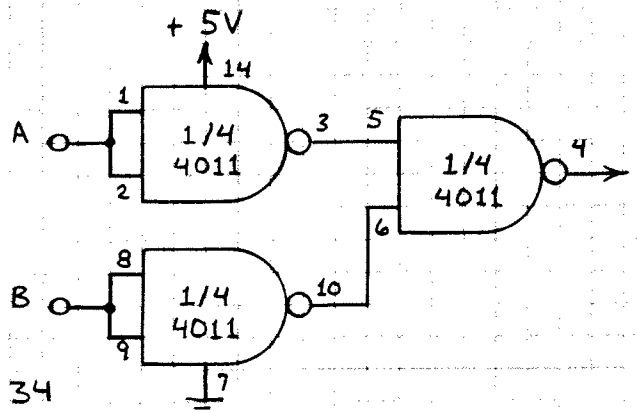
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

AND GATE



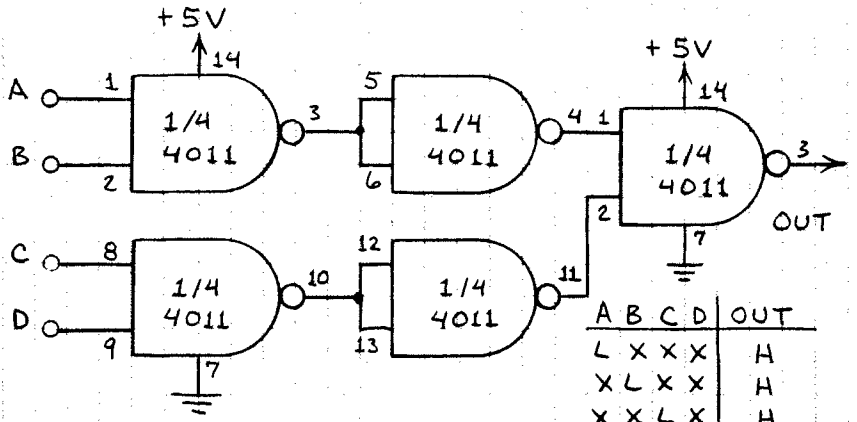
A	B	OUT
L	L	L
L	H	L
H	L	L
H	H	H

OR GATE



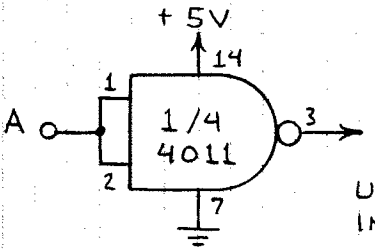
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	H

4-INPUT NAND GATE



A	B	C	D	OUT
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

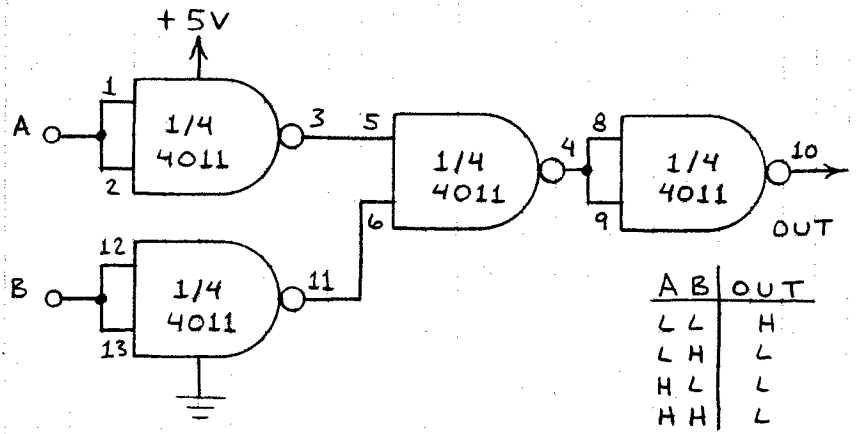
INVERTER



A	OUT
L	H
H	L

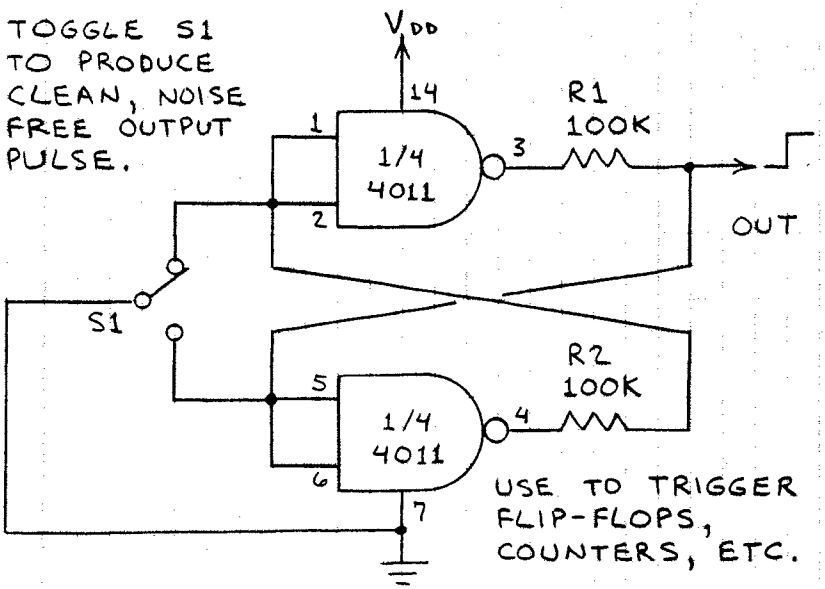
USE WHEN STANDARD INVERTER UNAVAILABLE.

NOR GATE

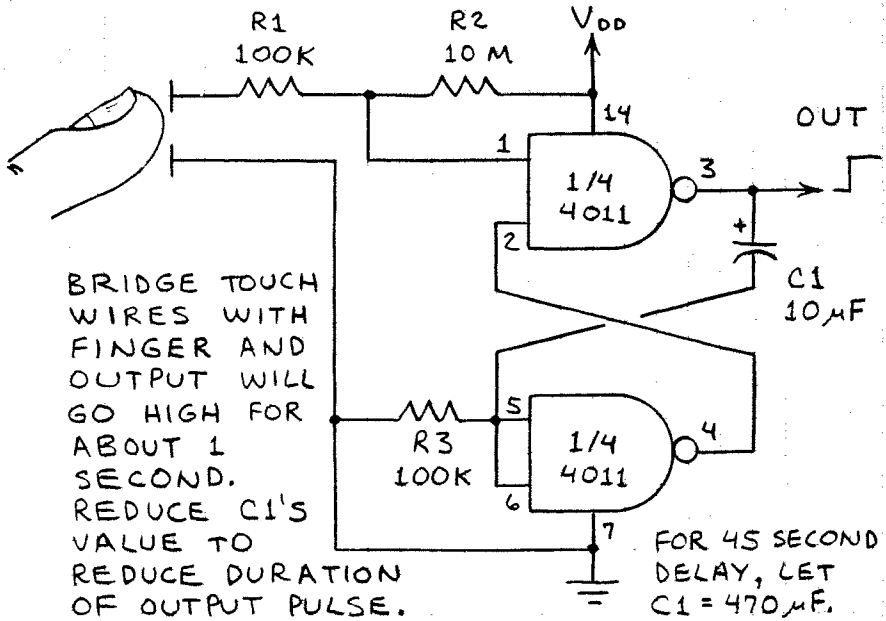


A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

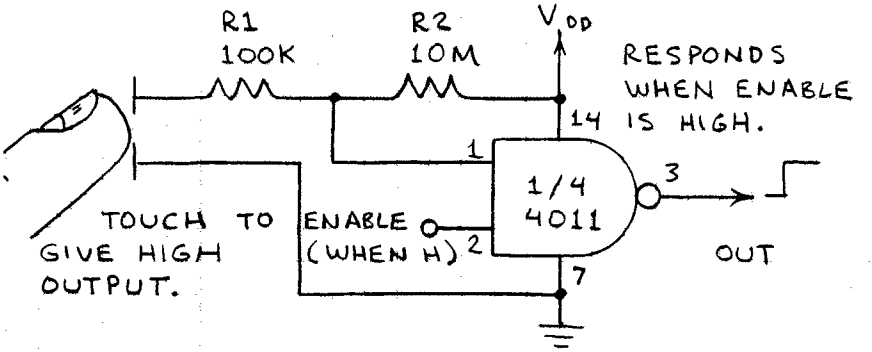
SWITCH DEBOUNCER



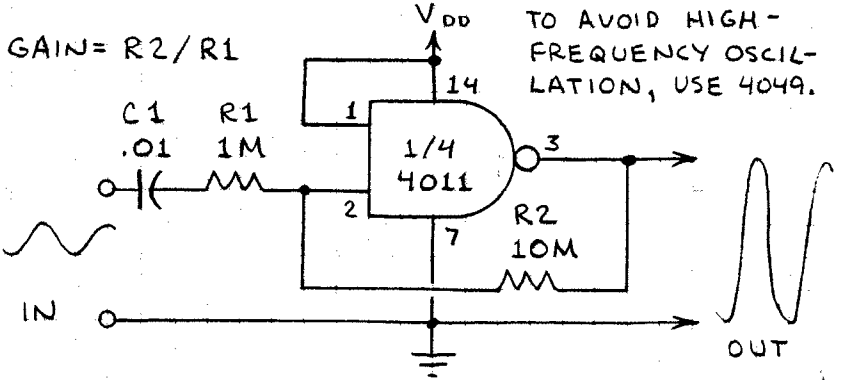
ONE-SHOT TOUCH SWITCH



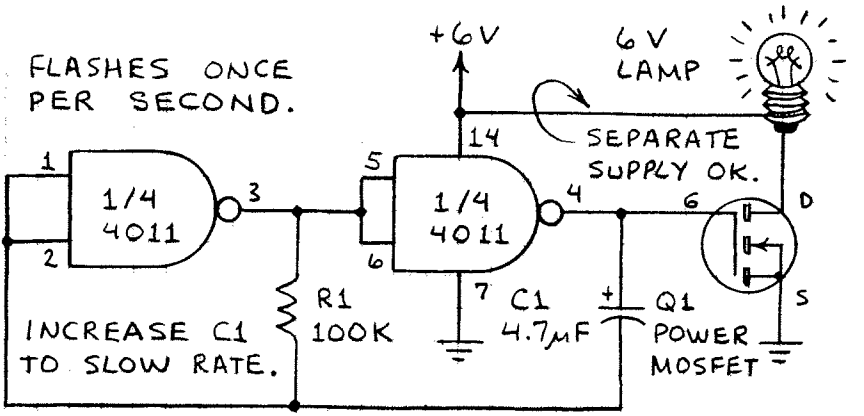
STANDARD TOUCH SWITCH



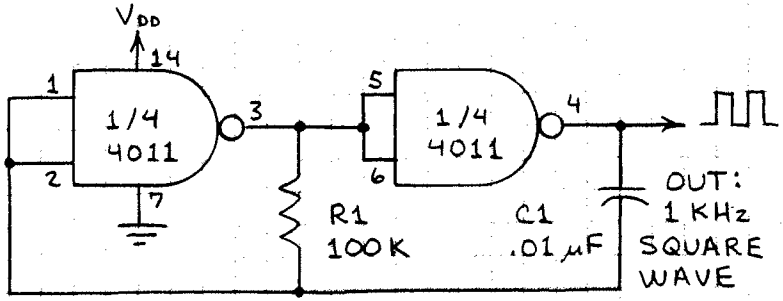
X-10 LINEAR AMPLIFIER



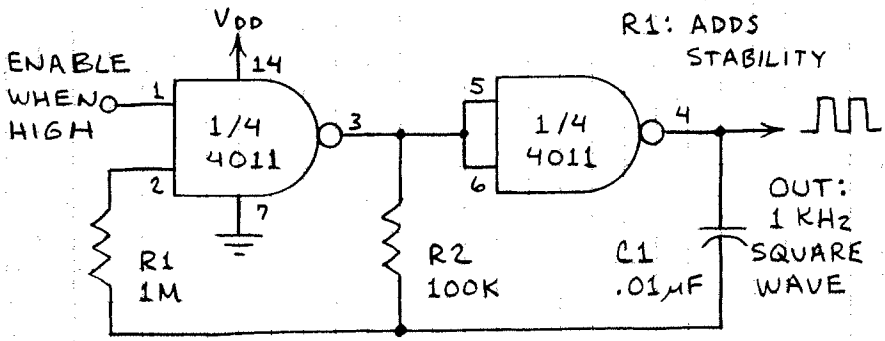
LAMP FLASHER



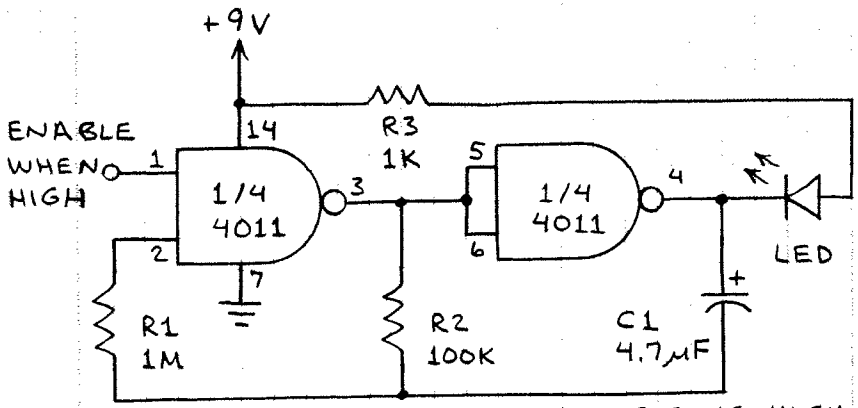
SIMPLE OSCILLATOR



GATED OSCILLATOR

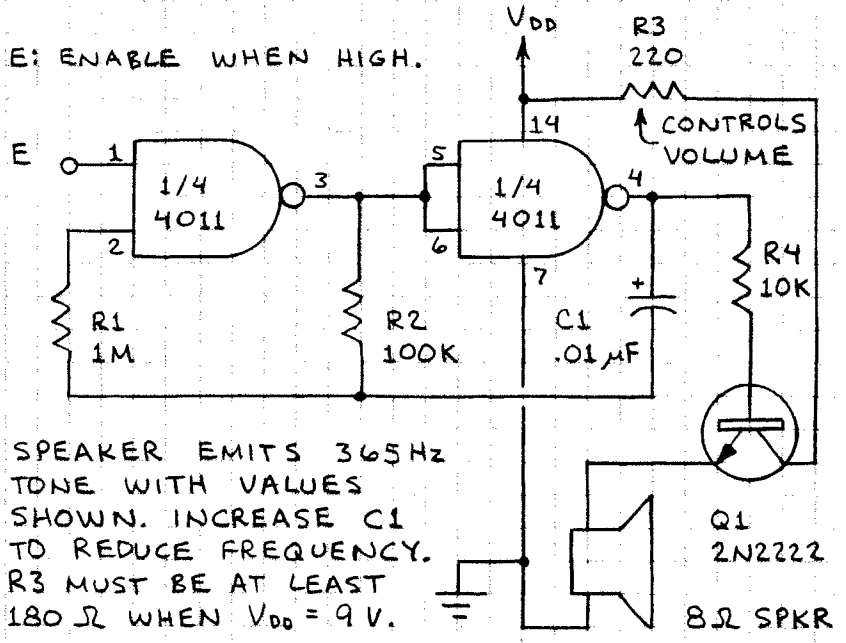


GATED LED FLASHER

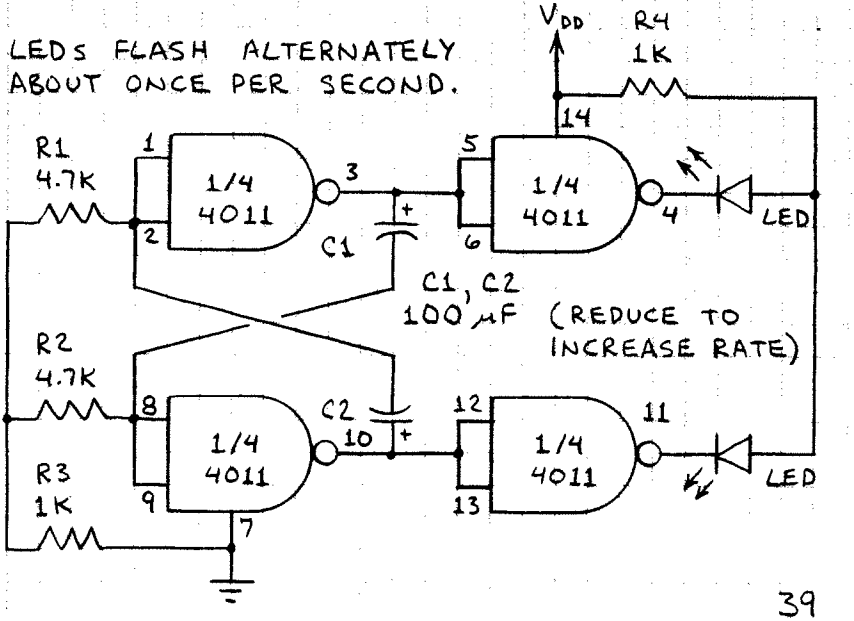


LED FLASHES 1-2 Hz WHEN ENABLE IS HIGH AND GLOWS CONTINUALLY WHEN ENABLE IS LOW.

GATED TONE GENERATOR



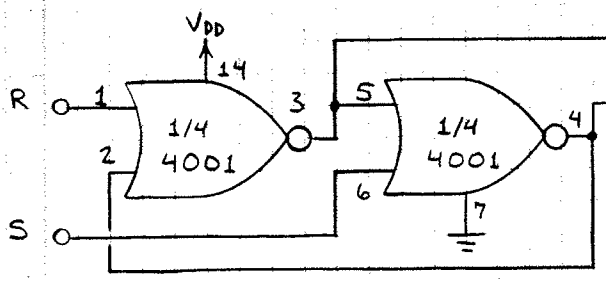
DUAL LED FLASHER



CMOS APPLICATION CIRCUITS

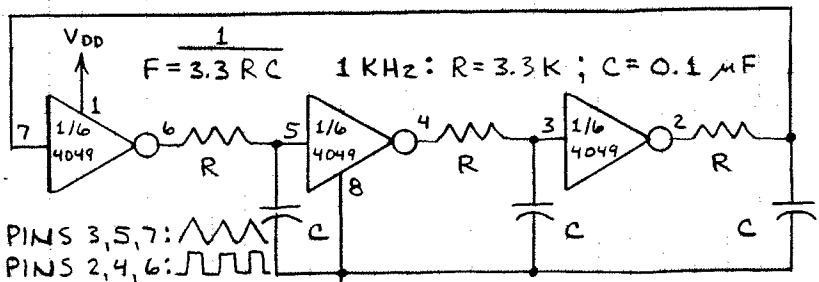
THE FOLLOWING CIRCUITS ILLUSTRATE THE VERSATILITY OF CMOS LOGIC CHIPS. ALL UNUSED INPUT PINS MUST GO TO V_{DD} OR GROUND.

RS LATCH



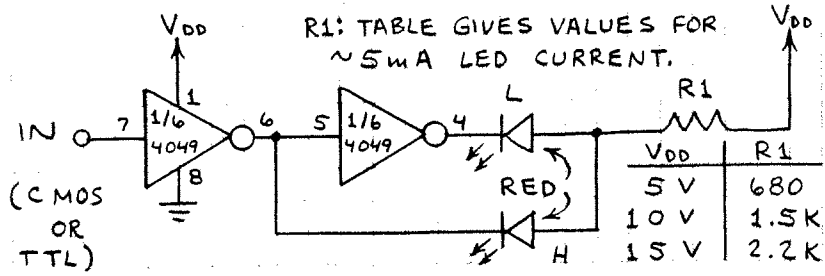
R	S	Q	Q̄
L	L	NO CHANGE	
L	H	H	L
H	L	L	H
H	H	DISALLOWED	

PHASE-SHIFT OSCILLATOR



USE 3/4 4011 FOR LESS CURRENT DRAIN. 4011 GIVES BETTER ⎍⎍⎍.

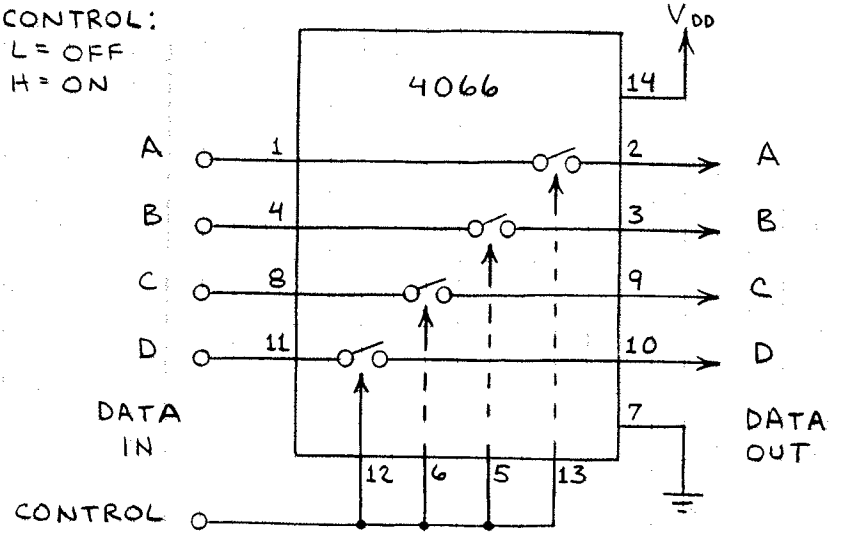
LOGIC PROBE



V_{DD}	R1
5 V	680
10 V	1.5K
15 V	2.2K

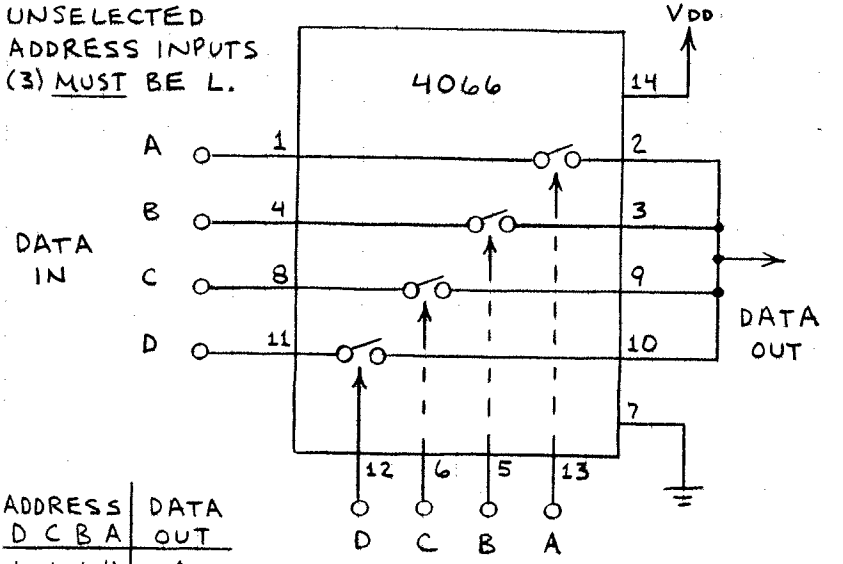
4-BIT DATA BUS CONTROL

CONTROL:
L = OFF
H = ON



1-OF-4 DATA SELECTOR

UNSELECTED ADDRESS INPUTS (3) MUST BE L.



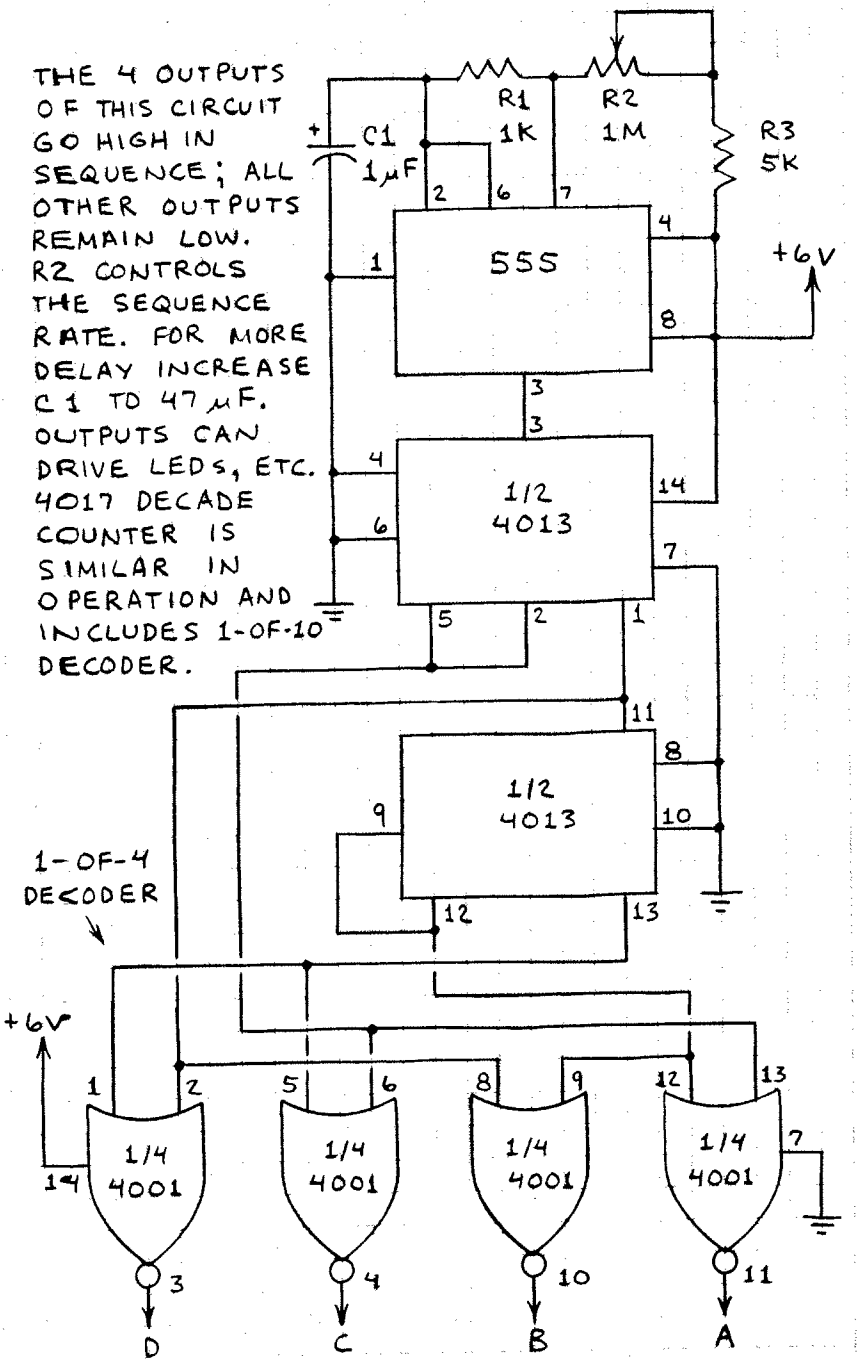
ADDRESS D C B A	DATA OUT
L L L H	A
L L H L	B
L H L L	C
H L L L	D

DATA SELECT (ADDRESS IN)

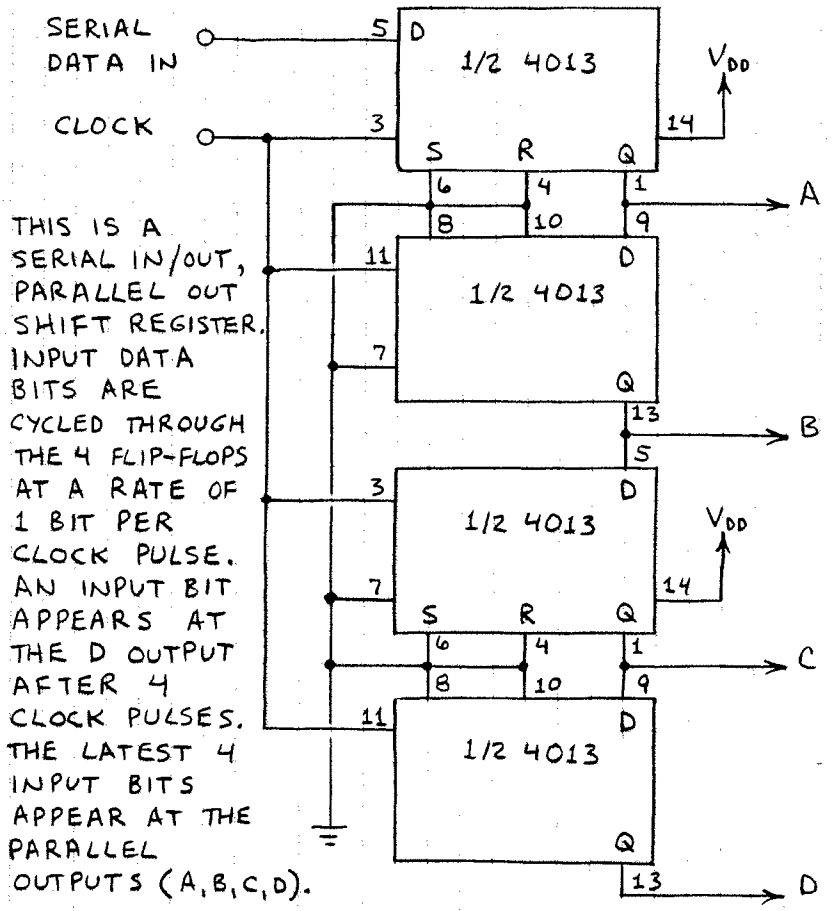
ONLY THE SELECTED ADDRESS CAN BE H.

1-OF-4 SEQUENCER

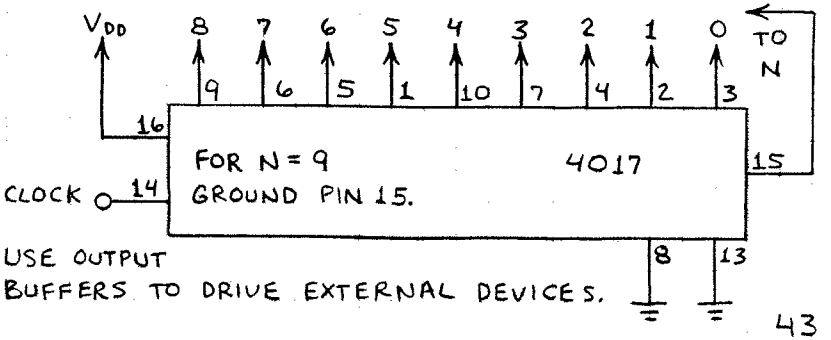
THE 4 OUTPUTS OF THIS CIRCUIT GO HIGH IN SEQUENCE; ALL OTHER OUTPUTS REMAIN LOW. R2 CONTROLS THE SEQUENCE RATE. FOR MORE DELAY INCREASE C1 TO 47 µF. OUTPUTS CAN DRIVE LEDs, ETC. 4017 DECADE COUNTER IS SIMILAR IN OPERATION AND INCLUDES 1-OF-10 DECODER.



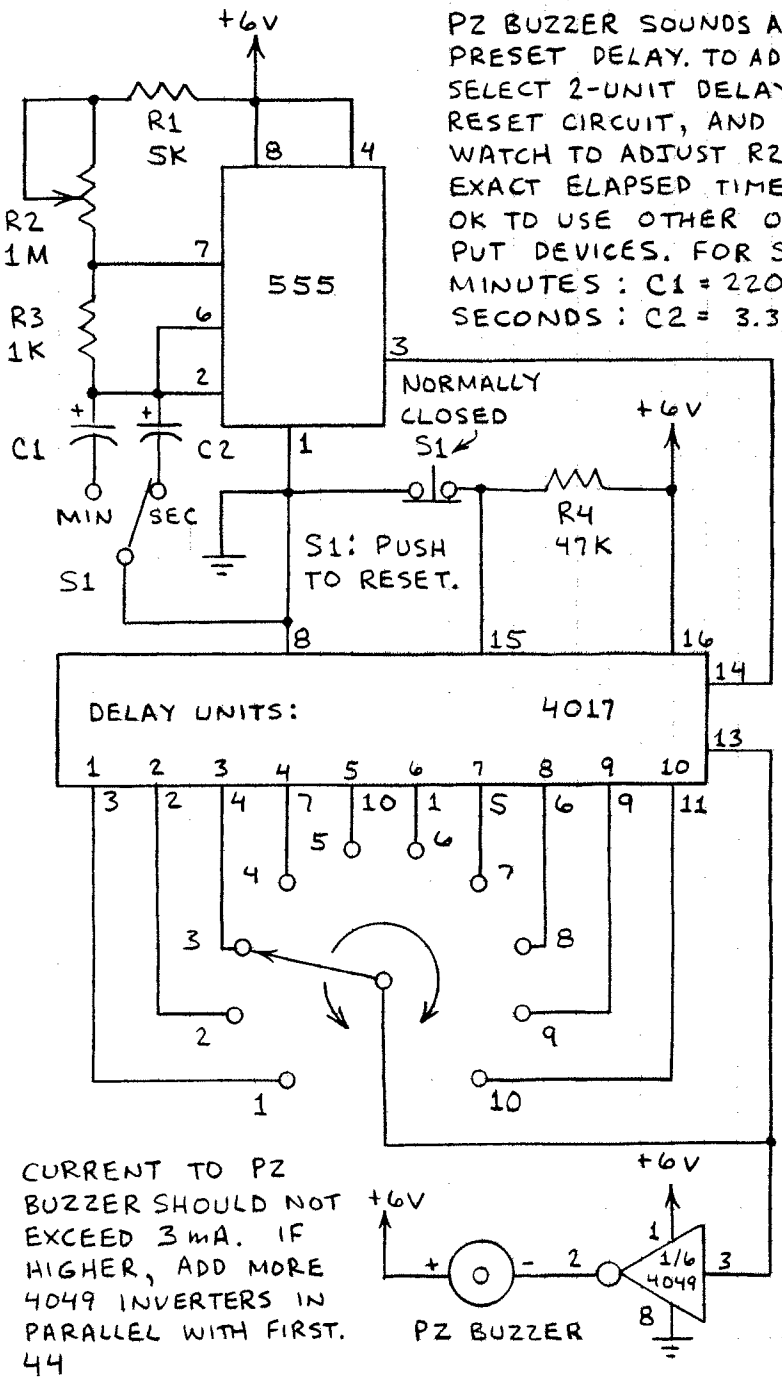
SHIFT REGISTER



COUNT TO N AND RECYCLE



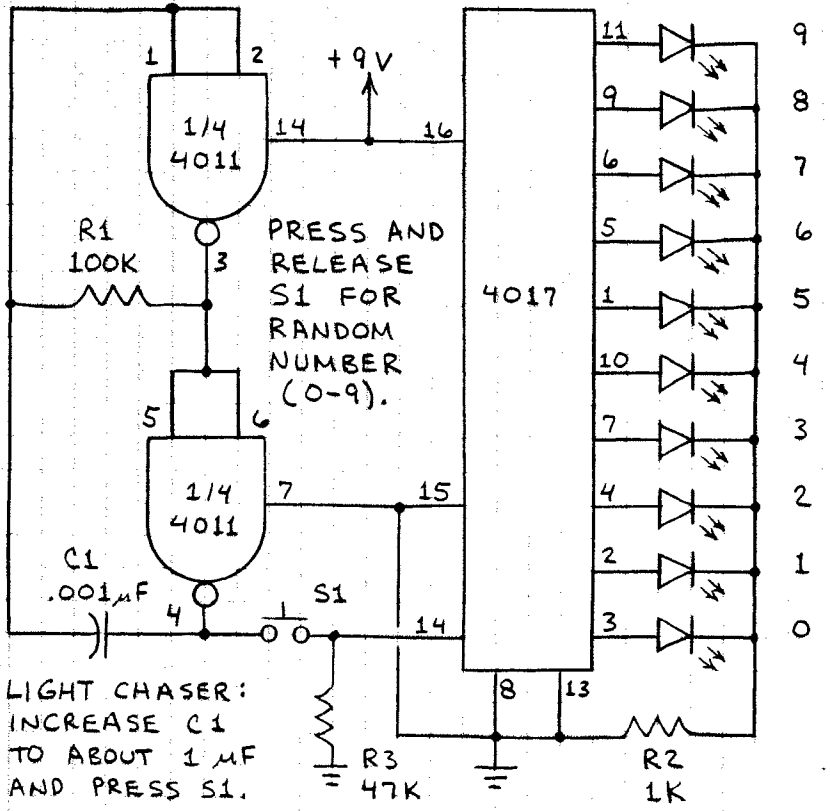
PROGRAMMABLE TIMER



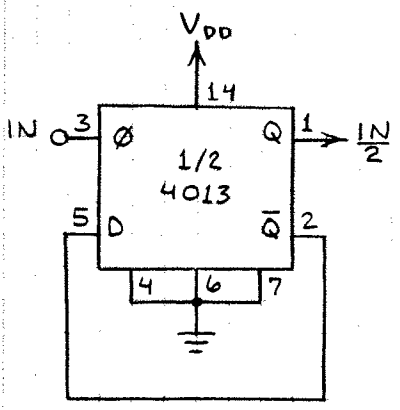
PZ BUZZER SOUNDS AFTER PRESET DELAY. TO ADJUST, SELECT 2-UNIT DELAY, RESET CIRCUIT, AND USE WATCH TO ADJUST R2 FOR EXACT ELAPSED TIME. OK TO USE OTHER OUTPUT DEVICES. FOR S1—
MINUTES : C1 = 220μF
SECONDS : C2 = 3.3μF

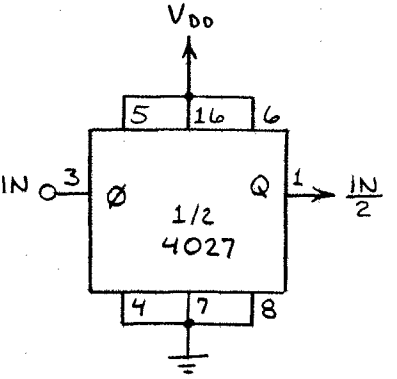
CURRENT TO PZ BUZZER SHOULD NOT EXCEED 3 mA. IF HIGHER, ADD MORE 4049 INVERTERS IN PARALLEL WITH FIRST.

RANDOM NUMBER GENERATOR



DIVIDE-BY-TWO COUNTERS

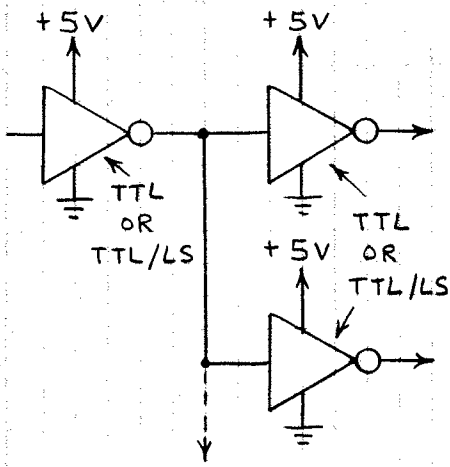




LOGIC FAMILY INTERFACING

THESE GUIDELINES PERMIT TTL AND CMOS LOGIC CIRCUITS TO BE INTERCONNECTED.

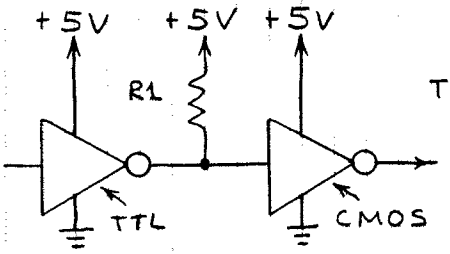
TTL TO TTL



TTL ⟶ 10 TTL
TTL ⟶ 20 TTL/LS
TTL/LS ⟶ 5 TTL
TTL/LS ⟶ 10 TTL/LS

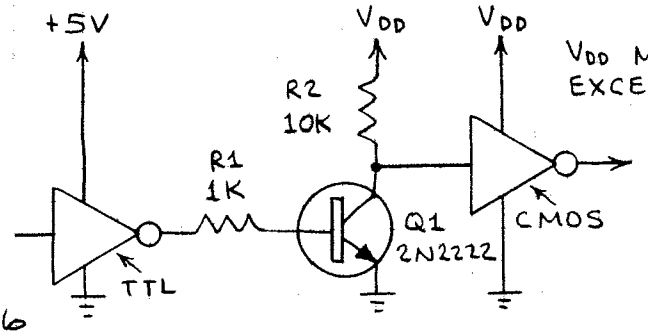
AVOID LONG INTERCONNECTION LEADS. USE BYPASS CAPACITORS TO DECOUPLE POWER SUPPLY NOISE (P.10).

TTL TO CMOS



TTL: R1 = 470-4.7K
TTL/LS: R1 = 1K-10K

NOTE THAT SUPPLY VOLTAGES ALL EQUAL 5V.

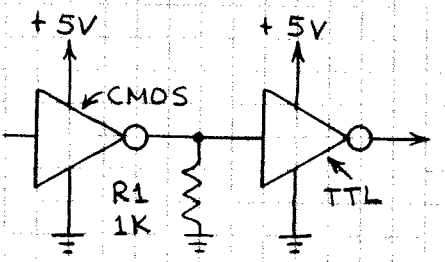


V_{DD} MAY EXCEED 5V.

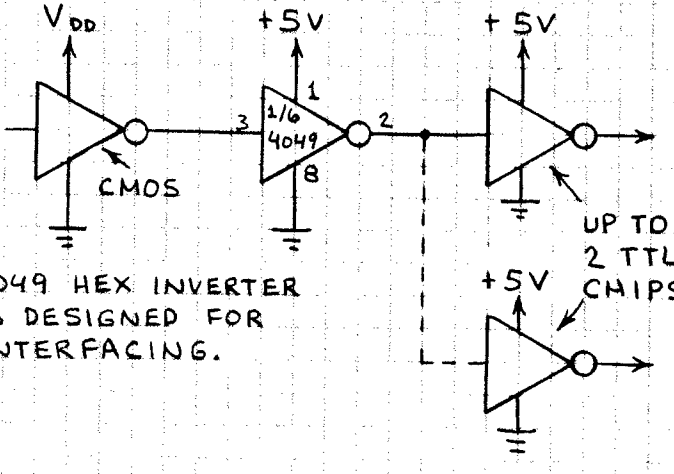
CMOS TO CMOS

A CMOS GATE OUTPUT CAN DRIVE UP TO 50 CMOS INPUTS. AVOID LONG INTERCONNECTIONS AND CONNECT <u>ALL</u> UNUSED INPUTS TO V_{DD} OR GROUND.

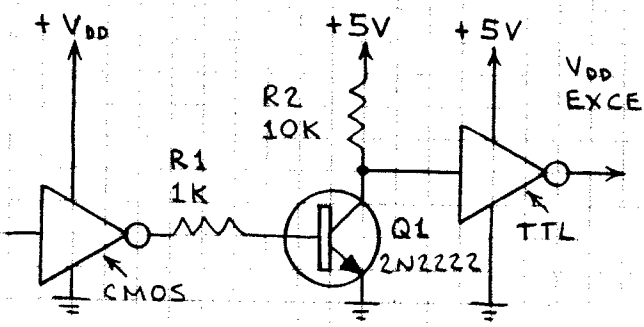
CMOS TO TTL



IF POSSIBLE, CHECK LOGIC INTERFACES WITH A LOGIC PROBE TO MAKE SURE THEY WORK AS INTENDED.



4049 HEX INVERTER IS DESIGNED FOR INTERFACING.



V_{DD} MAY EXCEED 5 V.

DIGITAL LOGIC TROUBLESHOOTING

SOMETIMES A DIGITAL LOGIC CIRCUIT MAY FAIL TO OPERATE OR MAY OPERATE IMPROPERLY. THE TROUBLESHOOTING PROCEDURES GIVEN HERE WILL ENABLE THE SOURCE OF MOST PROBLEMS TO BE IDENTIFIED. A LOGIC PROBE IS VERY HELPFUL WHEN TESTING A LOGIC CIRCUIT. USE A COMMERCIAL UNIT OR BUILD YOUR OWN.

1. REMOVE POWER FROM THE CIRCUIT.

2. CHECK ALL WIRING CONNECTIONS.

3. ARE ANY CHIP PINS BENT AND NOT FULLY INSERTED IN THE SOCKET OR CIRCUIT BOARD?

4. ARE ALL SOLDER CONNECTIONS GOOD?

5. DO ALL INPUTS GO SOMEWHERE? EVEN INPUTS OF UNUSED CMOS GATES MUST GO TO V_{DD} OR GROUND.

6. DOES THE CIRCUIT OBEY ALL OPERATING REQUIREMENTS (SUPPLY VOLTAGE, ETC.)?

7. DOES THE CIRCUIT INCLUDE DECOUPLING CAPACITORS CLOSE TO AND ACROSS THE SUPPLY PINS OF EVERY FEW CHIPS?

8. ARE THE INPUTS AND OUTPUTS OF ALL LOGIC CHIPS PROPERLY INTERFACED?

IF THESE STEPS DO NOT ISOLATE THE SOURCE OF THE PROBLEM, ONE OR MORE LOGIC CHIPS MAY BE DEFECTIVE. REMEMBER THAT CMOS CHIPS ARE ESPECIALLY VULNERABLE TO STATIC ELECTRICITY AND IMPROPER INPUT AND OUTPUT LOADING. FINALLY, BE SURE THE POWER SUPPLY WORKS PROPERLY AND IS CAPABLE OF PROVIDING SUFFICIENT CURRENT TO THE CIRCUIT IT POWERS.

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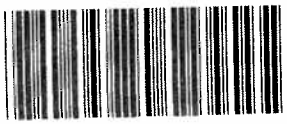
A Division of Tandy Corporation
Fort Worth, TX 76102
PRINTED IN U.S.A.



62-5014